

A NEW FAMILY OF DC-DC-AC POWER ELECTRONICS CONVERTERS

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TABLE OF CONTENTS

	Page
LIST OF TABLES	v
LIST OF FIGURES	vi
ABSTRACT	x
1 INTRODUCTION	1
1.1 Motivation	1
1.2 Literature Review	1
1.2.1 Applications	1
1.2.2 Single-phase Power Conversion Systems	2
1.2.3 Three-phase Power Conversion Systems	7
1.2.4 Single-phase to Three-phase Power Conversion Systems	11
1.2.5 Three-phase Four-wire Power Conversion Systems	13
1.3 Objectives	14
1.4 Thesis Organization & Technical Publications	15
1.4.1 Thesis Organization	15
1.4.2 Technical Publications	16
2 SINGLE-PHASE NON-ISOLATED BIDIRECTIONAL DC-DC-AC CON- VERTER	17
2.1 Model of the Converter	17
2.2 PWM Strategy	20
2.3 Control Strategy	21
2.4 Dc-link Capacitor Variables	23
2.5 Simulated Results	25
3 BIDIRECTIONAL DC-DC-AC THREE-PHASE POWER CONVERTER	30
3.1 Model of the Converter	30

	Page
3.2 PWM Strategy	33
3.3 Control Strategy	36
3.4 Dc-link Capacitor Variables	37
3.5 Simulated Results	39
4 DC-DC-AC POWER CONVERTER FOR THREE-PHASE FOUR-WIRE WITH BIDIRECTIONAL CHARACTERISTICS	48
4.1 Model of the Converter	48
4.2 PWM Strategy	51
4.3 Control Strategy	52
4.4 Dc-link Capacitor Variables	54
4.5 Simulated Results	55
5 PROOF-OF-CONCEPT EXPERIMENTAL SETUP	66
5.1 DSP	66
5.2 Drivers & Integrating Board	69
5.3 Power Converter & Heat-Sink	71
5.4 Experimental Outcomes	72
5.4.1 Three-phase Power Converter	72
5.4.2 Three-phase Four-wire Power Converter	73
6 CONCLUSIONS & FUTURE WORK	85
6.1 Conclusions	85
6.2 Future Work	86
LIST OF REFERENCES	88

LIST OF TABLES

Table	Page
2.1 Indication of prohibited switching states of three-switch leg.	19
3.1 Indication of prohibited switching states of three-switch leg.	32
4.1 Prohibited switching states of three-switch leg.	50

LIST OF FIGURES

Figure	Page
1.1 Bidirectional single-phase converter.	3
1.2 Circuit scheme of PFC converter.	4
1.3 SZMC topology.	5
1.4 Two-level AC-DC-AC single-phase converter	6
1.5 Flying capacitor multilevel inverter.	8
1.6 Bidirectional three-phase converter with eight switches.	8
1.7 Boost three-phase converter.	9
1.8 Topology of the Z-source inverter	10
1.9 Topology of three-phase inverter with active power filter	11
1.10 Proposed topology with the buffer system and active power filter.	12
1.11 Proposed topology for single-phase to three-phase system	12
1.12 Proposed topology for three-phase to single-phase system	13
1.13 Voltage and frequency controller	14
2.1 Single-phase non-isolated bidirectional DC-DC-AC converters: (a) conventional and (b) proposed solutions.	18
2.2 PWM strategy: single-phase converter.	22
2.3 THD of the output current as a function of m_a	22
2.4 Control block diagram.	23
2.5 dc-link capacitor current versus frequency using triangular: (a) Conventional topology (b) Proposed topology	24
2.6 Simulation results for the single-phase converter: (a) reference and measured capacitor voltages, and (b) reference and measured dc currents.	26
2.7 Simulation results for the single-phase converter: (a) voltage at ac converter side, and (b) current at ac converter side.	27

Figure	Page
2.8 Simulation results for the single-phase converter: (a) reference and measured capacitor voltages, and (b) reference and measured dc currents. .	28
2.9 Simulation results for the single-phase converter: (a) voltage at ac converter side, and (b) current at ac converter side.	29
3.1 Bidirectional converter interfacing DG system, hybrid dc and ac micro-grid: (a) conventional solution with eight switches, (b) proposed solution with seven switches and	31
3.2 (a) PWM strategy, and (b) reference voltage: v_{1i0}^* , v_{1o0}^* , v_{2o0}^* , v_{3o0}^* , v_{μ}^* , and V_{dc}^*	35
3.3 THD of the output current as a function of m_a	36
3.4 Control block diagram.	37
3.5 dc-link capacitor current versus frequency using triangular: (a) Conventional topology (b) Proposed topology	38
3.6 Three phase currents : (a) conventional topology, (b) proposed topology.	40
3.7 Simulation results for the three-phase conventional converter:(a) phase voltage at phase 1, (b) phase voltage at phase 2, and (c) phase voltage at phase 3.	41
3.8 Simulation results for the three-phase conventional converter: (a) line-line voltage (phase 1-2), (b) line-line voltage (phase 1-3), and (c) line-line voltage (phase 2-3).	42
3.9 Simulation results for the three-phase proposed converter: (a) phase voltage at phase 1, (b) phase voltage at phase 2, and (c) phase voltage at phase 3.	43
3.10 Simulation results for the three-phase proposed converter: (a) line-line voltage (phase 1-2), (b) line-line voltage (phase 1-3), and (c) line-line voltage (phase 2-3).	44
3.11 Simulation results for the three-phase conventional converter: (a) reference and measured capacitor voltages, and (b) reference and measured dc currents.	45
3.12 Simulation results for the three-phase proposed converter: (a) reference and measured capacitor voltages, and (b) reference and measured dc currents	46
3.13 Simulation results for the three-phase converter: (a) transient operation for the reference and measured currents , (b) transient operation for the reference and measured capacitor voltages	47

Figure	Page
4.1 Bidirectional DC-DC-AC converters : (a) conventional solution, and (b) proposed converter.	49
4.2 (a) Analog PWM strategy, (b) THD of the output current as a function of m_a	53
4.3 Control block diagram.	54
4.4 Spectrum of the dc-link capacitor current: (a) conventional and (b) proposed topology.	56
4.5 Three-phase ac currents: (a) conventional topology and, (b) proposed topology.	57
4.6 Simulation results for the three-phase conventional converter: (a) phase voltage at phase 1, (b) phase voltage at phase 2, and (c) phase voltage at phase 3.	59
4.7 Simulation results for the three-phase conventional converter: (a) line-line voltage (phase 1-2), (b) line-line voltage (phase 1-3), and (c) line-line voltage (phase 2-3).	60
4.8 Simulation results for the three-phase conventional converter: (a) reference and measured capacitor voltages, and (b) reference and measured dc currents.	61
4.9 Simulation results for the three-phase proposed converter: (a) phase voltage at phase 1, (b) phase voltage at phase 2, and (c) phase voltage at phase 3.	62
4.10 Simulation results for the three-phase proposed converter: (a) line-line voltage (phase 1-2), (b) line-line voltage (phase 1-3), and (c) line-line voltage (phase 2-3).	63
4.11 Simulation results for the three-phase proposed converter: (a) reference and measured capacitor voltages, and (b) reference and measured dc currents.	64
4.12 Simulation results for the three-phase converter: (a) transient operation for the reference and measured currents, and (b) transient operation for the reference and measured capacitor voltages	65
5.1 Photo of the Printed Circuit Board for the starter kit.	67
5.2 Spectrum of code composer: (a) code composer studio setup, (b) connect the board and (c) open the project.	68
5.3 Spectrum of code composer: (a) build the project, (b) load the program and (c) run the program.	74

Figure	Page
5.4 Driver 2SC0108T.	75
5.5 Spectrum the 2SC0108T driver sides: (a) Primary side, (b) Secondary side.	75
5.6 Basic board 2BB0108T.	76
5.7 Primary and Secondary sides of the basic board 2BB0108T.	76
5.8 Integrated board.	76
5.9 Spectrum of power parts: (a) BSM75GB60DLC IGBT module, (b) DC source and (c) Snubber capacitor.	77
5.10 Spectrum of power parts: (a) Dc-link capacitor, (b) Heat sink and (c) Three-phase load.	78
5.11 (a), PWM for the leg with three switches, (b) and (c) Proposed three-phase converter.	79
5.12 Experimental results for proposed three-phase converter: (a) v_{1b0} and i_{ac1} , (b) v_{1a0} and i_{ac1} , (c) v_{20} and i_{ac2} , and (d) v_{30} and i_{ac3}	80
5.13 Experimental results for three-phase proposed converter: (a) v_{1a0} and I_{dc} , (b) v_{1a2} and i_{ac1} and (c) v_{ac3} and i_{ac3}	81
5.14 Experimental results for three-phase with four-wire converter: (a) line-line voltage v_{13} and phase current i_{ac1} and (b) average of the current and voltage	82
5.15 Experimental results for three-phase with four-wire converter: (a) phase voltage v_{ac1} and phase current i_{ac1} (b) average of the voltage and current	83
5.16 Experimental results for three-phase with four-wire converter: (a) V_{1b0} and the i_{1a-1b} and (b) V_{1b0} and the phase current i_{ac1}	84

ABSTRACT

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This thesis proposes a family of non-isolated bidirectional converter in order to interface dc and ac variables. Such power electronics solutions guarantee: (i) bidirectional power flow between dc and ac converter sides, (ii) independent control in both converter sides, (iii) high level of integration with a reduction of one power switch and its drive circuits, (iv) implementation of two functions by using a unique power conversion stage and (v) reduction of the capacitor losses. Despite proposing new power converter solutions, this thesis presents an analysis of the converters in terms of pulse-width-modulation (PWM) strategy, dc-link capacitor variables, and suitable a control approach.

Solutions for single-phase, three-phase and three-phase four-wire systems are proposed by employing a converter leg with three switches. A possible application of this converter is in Vehicle-to-Grid (V2G) systems and interfacing dc microgrid with a utility grid.

In addition to the new power electronics converters proposed in this thesis, an experimental setup has been developed for validation of the simulated outcomes. The proof-of-concept experimental setup is constituted by: DSP, Drivers & Integrating Board, Power Supply and, Power Converter & Heat-Sink .

1. INTRODUCTION

1.1 Motivation

Power electronics converters play an essential role interfacing electrical sources and loads in systems dealing with energy conversion, such as renewable energy systems and hybrid/electrical vehicles. Most of the applications employing power converters require higher power capability while maintain a compact size, which implies in extremely challenging requirements for high power density.

The motivation to develop this thesis lies on the proposition of new power electronics solutions with higher level of integration by reducing the number of power semiconductor devices along with its driver circuitry, while maintain the same characteristics of the conventional converters.

1.2 Literature Review

In this section, existing papers dealing with; 1) single-phase, 2) three-phase, 3) single-phase to three-phase, 4) three-phase to single-phase, and 5) three-phase four-wire power converters are summarized. Before presenting the energy conversion units mentioned earlier, it will be furnished some applications where such power electronics converters can be applied.

1.2.1 Applications

A state-of-the-art related to power electronics converters applied to micro grid, V2G systems and any power system applications needing to convert DC-DC, DC-AC, AC-DC and AC-AC will be presented in this section.

A micro-grid can be defined as a localized grouping of electricity generation, energy storage, and loads that normally operate connected to a traditional centralized grid (macro-grid). The interface between micro- and macro-grid is possible due to development reached by the power electronics field, and an important equipment in this scenario is the Energy-Control-Center (ECC), composed of a bidirectional AC-DC (or DC-AC) power conversion converter used to interface the utility ac grid and dc-link [1,2]. The multiple dispersed generation sources and the ability to isolate the micro-grid from a larger network would provide highly reliable electric power [3,4]. The multiple applications for single-phase to three-phase power converter described in [5–7], which mostly they applicable in a rural applications. The work presented in [8,9] brings a state-of-the-art of non isolated bidirectional DC-DC converters for applications in hybrid electric vehicles. In [10] a bidirectional inverter was presented that is connected in parallel to the utility system, operating as an uninterruptible power supply.

1.2.2 Single-phase Power Conversion Systems

A direct solution of DC-DC-AC single-phase converter consists of a bidirectional DC-DC converter connected to a two-leg converter (H-bridge topology) through a dc-link capacitor, made up of six power switches, as presented in [1]. This kind of converter has direct application in vehicle to grid (V2G) system and interfacing a dc-link micro-grid system with a single-phase utility grid as shown in Fig. 1.1.

The interface between micro-generators and micro-grids with the macro-grid is possible due to developments in the power electronics field. Much of this development focuses on efficiently converting AC power to another form of AC power. The authors of [11] presented an SPMC algorithm that allows a single phase power converter to act as a frequency changer, rectifier, inverter, or chopper.

An important subject in AC-AC power converters is power factor correction (PFC), which determines how efficiently power is converted from the AC source to

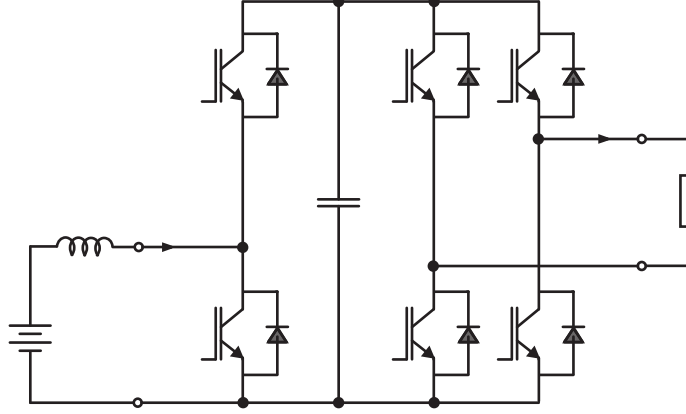


Fig. 1.1. Bidirectional single-phase converter.

the AC load. The authors of [12] discussed many single-stage converter topologies which were capable of optimizing the power-factor. These comparisons were based on the AC source frequency, DC-link capacitor usage, and the type of control algorithm. Ultimately, the best topology will be determined by the application. The authors of [13] presented a modified sinusoidal PWM (SPWM) switching technique to optimize the power factor of an AC-AC converter by shifting the delayed current to be in phase with the grid voltage as shown in Fig. 1.2. The advantage of the SPWM switching technique is the fact that compensation capacitors can be avoided, which improves power efficiency. The authors of [14] presented a two-stage PFC configuration which uses both active and passive techniques to improve power factor. This hybrid mode PFC design has a higher conversion efficiency than a conventional two-stage PFC configuration and additionally lowers the stresses on the switches and bulk capacitor. Similarly, the authors of [15] presented a steady-state analysis of a soft-switching PFC converter which uses an active snubber cell to reduce stresses on the main and auxiliary switches. The 100 kHz, 300 W prototype was tested to show that the efficiency of the converter is 98% and the power factor was 0.99.

The soft-switching technique used in [15] is explored in other papers because soft-switching reduces voltage stresses and increases converter life. The author of [16] applied a zero voltage switching (ZVS) strategy to a AC-DC-AC converter. The

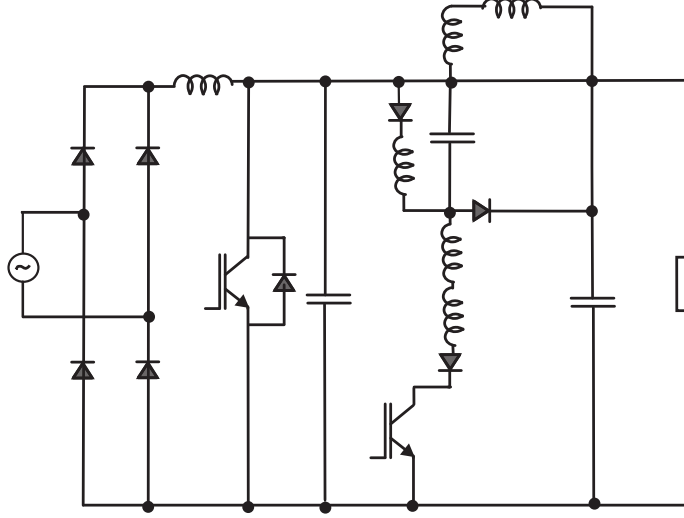


Fig. 1.2. Circuit scheme of PFC converter.

rectifier of the design uses a single converter and an average-current mode control scheme to deliver low harmonic, high power factor input current. The inverter of the design uses sinusoidal PWM to achieve dynamic regulation that delivers stable AC voltage. Quasi-Z-source converters are another topology that is used to improve power factor. The authors of [17–19] presented new topologies of quasi-Z-source AC-AC converters as depicted in Fig. 1.3. The converter in [17] operates in continuous current mode while the input voltage and output voltage share the same ground. This converter can operate as buck-boost or reversing converter while maintaining phase angle. The lab prototype showed an improved input power factor and lower input current THD than a conventional impedance source AC-AC converter design. In [18] the authors presented a converter design which employed a safe commutation strategy to reduce stress on the switched and avoid voltage spikes. In [19] the authors presented a Z-source buck-boost matrix converter which again uses a safe-commutation strategy to eliminate voltage spikes without using a snubber circuit. These topologies can be used to increase or decrease the output voltage amplitude and frequency.

The Z-source converter topology can also be used to reduce the number of switches in a power supply. The authors of [20] presented voltage and current-fed Z-Source

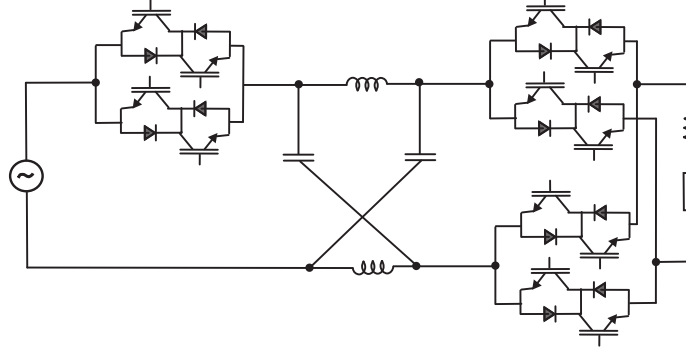


Fig. 1.3. SZMC topology.

converters which only use two switches to achieve AC-AC power conversion. The converter can still be used for buck-boost or reversing and maintaining phase-angle. The converter presented uses PWM duty-ratio control to essentially create solid-state transformers.

Several types of control techniques have been applied to AC-AC converters. The authors of [21] used a sliding mode controller to improve regulation, sensitivity, and transient response for a AC-AC quantum resonant converter. The paper presents a model for the resonant converter and describes the sliding mode control scheme. The authors of [22] presented a PWM strategy to balance the DC-link voltage of a three level, three leg AC-DC-AC converter as depicted in Fig. 1.4. In [23] the authors use a P-I control scheme to properly control an AC-AC converter which is used for an AC railway traction vehicle application. The controller can successfully operated with both a normal sinusoidal and highly disturbed line voltage source.

Many AC-AC power converters have a DC link in the topology; these types of converters essentially become an AC-DC rectifier followed by a DC-AC inverter. Many authors have presented new guidelines, topologies and controller designs for the AC-DC rectifier module of these power converters. The authors of [24] presented a study of harmonic instabilities which can occur AC-DC power systems because of switch commutation time. The paper suggests some guidelines for effectively overlapping initialization angles in order to avoid harmonic instabilities. The authors of [25] pre-

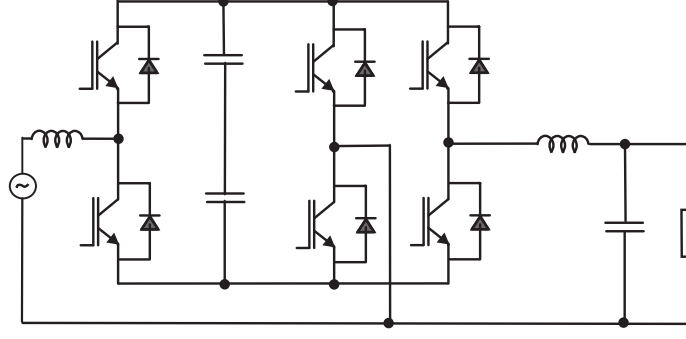


Fig. 1.4. Two-level AC-DC-AC single-phase converter

sented a rectifier topology in which a bi-directional neutral point clamp is used to reduce voltage stress on the switches. The rectifier design employs an inner loop current controller, an outer loop current controller, and a voltage balance compensation controller. Experimental results show the converter drawing clean AC voltage with a unity power factor while regulating the output DC bus voltage. The authors of [26] presented a new rectifier topology which used one reverse blocking switch conducts at a time. A sliding-mode control of the input current achieves a high input power factor and low THD while reducing the size, weight, and cost of the DC inductor of the rectifier. A P-I controller regulates rectifier's voltage output.

Several authors have presented paper on how to optimize Power Factor Correction (PFC) in AC-DC rectifiers. The authors of [27] proposed a AC-DC converter which achieves PFC by detecting AC line voltage waveform. A boost chopper on the DC side of the converter is used to provide PFC while the circuit parameters are used to generate an AC current waveform. A feed forward control is implemented to line up the AC current wave form with the AC line voltage waveform. The authors of [28] proposed a transformer-less AC to high voltage DC converter which is a modified Cockcroft-Walton voltage multiplier circuit. The proposed topology uses an additional bi-directional switch along with a boost inductor to improve the power factor at the AC source and provide regulated DC output for a wide load range. The control strategy used a commercial IC which controls the average current of continuous

conduction to apply PFC. Instead of high voltage DC, the authors of [29] presented a two-stage power converter that produces low voltage DC from a wide range of high voltage AC input. The first stage is a buck/boost converter which uses PWM for PFC. The second stage used a PWM strategy to step down and regulate the low voltage DC output.

Many converter topologies and control schemes can be applied to inverters which convert renewable DC power into single phase AC grid power. The authors of [30] presented a new five-level design which is based on a full bridge converter. The design has an additional two power switched and diodes which are connected to the midpoint of the DC link. These additional switches are controlled by a PWM strategy to balance the midpoint voltage of the DC link. The authors of [31] presented a design to reduce the low frequency ripple that often appears on the DC side of inverters and shortens the lifetime of DC voltage sources. The design used a series, parallel feedback P-I controller in order to reduce DC current ripple in the inverter. A non-linear gain control scheme is employed to ensure that the output voltage over/under shoot stays in an acceptable range during step changes of the load.

Sometimes DC-DC converter topologies are used in single phase-single stage power converters. The authors of [32] presented a DC-DC converter that controls the DC link asymmetrically to achieve voltage quality enhancement. This strategy is used because by regulating the DC link voltage asymmetrically will improve the voltage quality of the output of some multi-level inverters as depicted in Fig. 1.5.

1.2.3 Three-phase Power Conversion Systems

The configuration presented in Fig. 1.6, which was proposed in [33,34], uses two power processing stages and can be used for both grid-connection and stand-alone applications. The authors of [35,36] used the single-reference-six-pulse modulation (SRSPM) to control the front-end DC-DC converter and employ 33% of the modulation to control the three-phase DC-AC inverter. The proposed converter doesn't

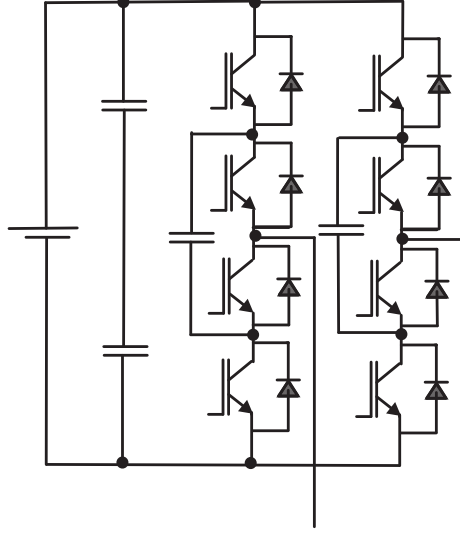


Fig. 1.5. Flying capacitor multilevel inverter.

need a dc-link capacitor, so the modulated information at the input of the three-phase inverter is retained.

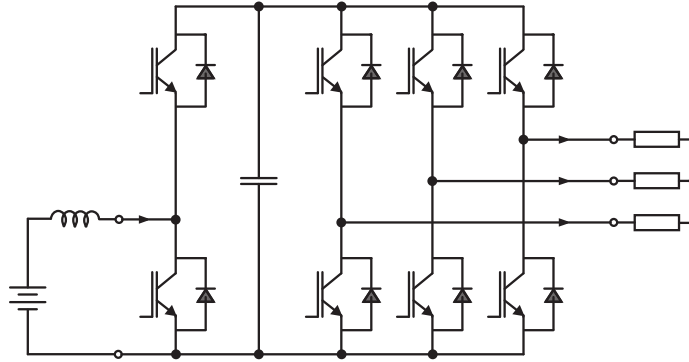


Fig. 1.6. Bidirectional three-phase converter with eight switches.

The three-phase boost converters presented in [37–40] employ a single stage DC-AC three phase power converter in order to convert the DC voltage to AC grid voltage. The authors used the one-cycle control (OCC) and the PWM method to convert the low DC voltage to high AC grid voltage by injecting three-phase current into the grid. This kind of simple converter, which is depicted in Fig. 1.7, reduces power losses.

In [41], a cascade H-Bridge multilevel boost inverter is proposed in order to convert the DC-AC without the bulky inductor. In this case, each H-Bridge needs its own DC power supply while a capacitor is used for the DC source. In [42,43], the authors proposed a three-phase DC-AC inverter for use with an unbalanced source and/or nonlinear loads. The proposed converter needs three additional ac power switches to obtain the three-level PWM. An additional circuit is added to the system to reduce distortion of the output voltage. The main advantages of the proposed converters are reduction of switching losses and elimination of electromagnetic interference.

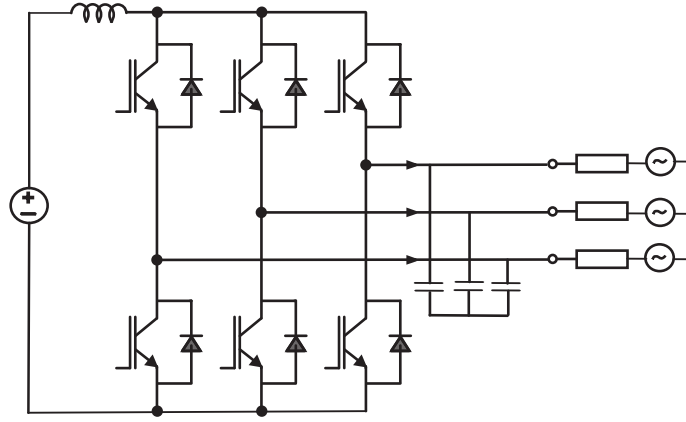


Fig. 1.7. Boost three-phase converter.

In [44–46], the authors proposed two three-level DC-AC cascade type Z-source buck-boost inverters. Unlike the traditional buck inverters, these inverters can step down or step up the voltage. As depicted in Fig. 1.8, the proposed inverters consist of two isolated DC sources and two cascade Z-sources. The mathematical model for the Z-source three-phase boost rectifier is presented while specifically analyzing the converter's power factor correction.

In [47], a AC-AC three-phase converter is proposed which implements a three-phase PWM. The control concept of the dc-link, back-to-back converter uses an indirect matrix converter (IMC) which used modulation to eliminate the dc-link capacitor.

While designing controllers for inverters, important features to consider are: low cost, simple control, fast response and independence from the load and switching

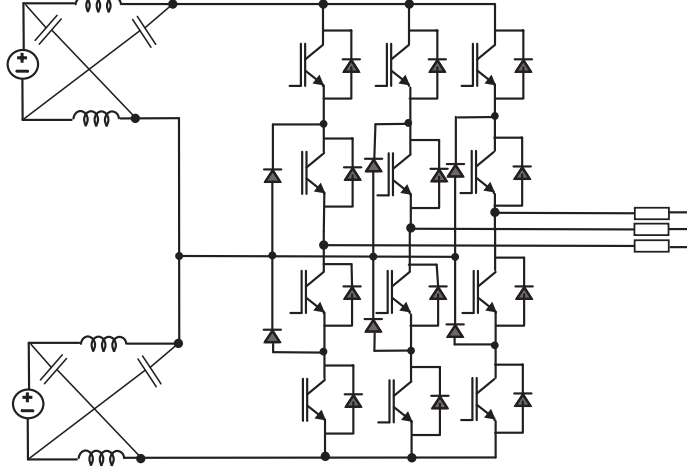


Fig. 1.8. Topology of the Z-source inverter

frequency. The work presented in [48, 49] proposed a novel simple control technique to control the output DC voltage of a three-phase AC-DC converter. Bidirectional power electronic converters have the ability to control voltage/current at both sides of converter. Bidirectional converters are crucial in distributed generation systems [50] such as smart-grids and micro-grids. In [51] a control scheme for a three-phase two-leg switching mode rectifier with a neutral-point clamp is proposed for ac line coordination. The inner loop of the controller tracks the ac current to produce unity power factor while the outer loop of the controller tracks the dc-bus voltage. In [52–54] a shunt power filter is added to a three-phase two leg voltage source in order to eliminate the harmonics. This inverter used a current controller to supply the active power and to compensate for inverter losses. The outer loop controls the dc-link voltage and the inner loop controls the ac input current for the AC-DC three-phase converter as shown in Fig. 1.9. In [55] the authors improved the power factor of a three-phase AC-DC converter by injecting a high frequency current which operates above the converters resonant frequency.

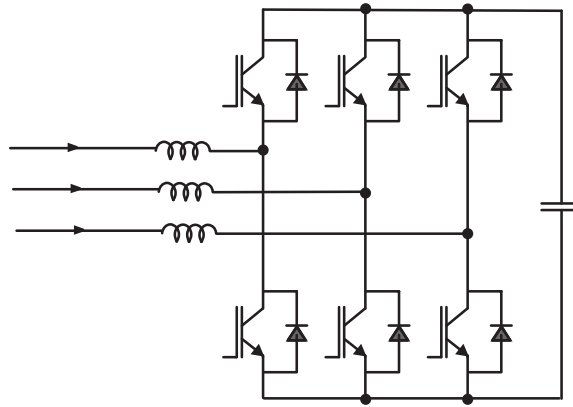


Fig. 1.9. Topology of three-phase inverter with active power filter

1.2.4 Single-phase to Three-phase Power Conversion Systems

The sources [56–58] presented a novel single-phase to three-phase power converter which does not require the use of a large dc-link capacitor or a large inductance reactor. A small capacitor is used to compensate for the reactive current from a generator; a larger capacitor is used to reduce the power ripple. In this case, an indirect-matrix-converter-with-buffering is the control scheme which decouples the power ripple as depicted in Fig. 1.10. In [59–64], the authors tested different kinds of single-phase to three-phase power converters, which either reduce or increase the number of electronic components of the converter. Both the proposed and conventional converters have the same features such as, sinusoidal currents, unity power factor and a control strategy for the dc-link voltage. These authors focused on improving the reliability, increasing the efficiency, and reducing distortion.

Two important failure modes for single-phase to three-phase AC-DC-AC converters are open-circuit and short-circuit faults. After analyzing these failure modes, the authors of [65, 66] proposed a new converter topology. The proposed converter employs isolation devices and connection devices to compensate for faults. Additionally, the proposed topology decreases harmonic at the input side of the converter and reduces the rectifier switch currents as shown in Fig. 1.11. The active power filter

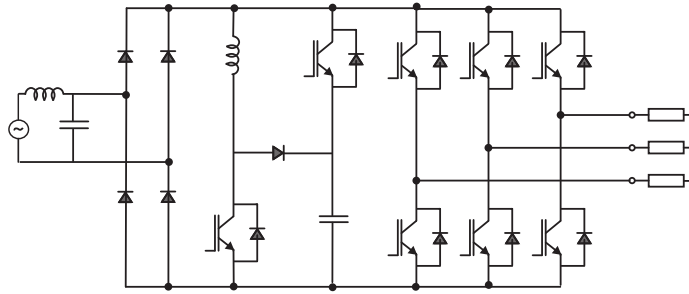


Fig. 1.10. Proposed topology with the buffer system and active power filter.

proposed for the single-phase to three-phase power converter in [67,68] eliminates the harmonics and reactive power. The authors of [69] analyze a single-phase to three-phase power converter operating under unbalanced, linear, and nonlinear loads. The authors then proposed a new converter topology based on their analysis.

The authors of [70] presented a single-phase to three-phase converter which can compensate for open-circuit or short-circuit faults. When a fault is detected the converter topology is modified by isolation and connection devices in order to maintain the same power rate as before the fault.

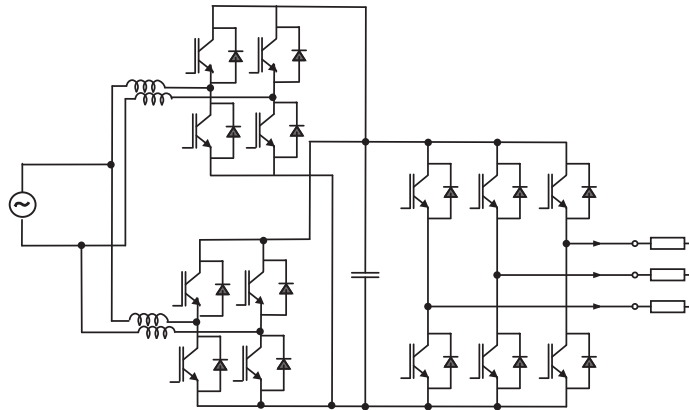


Fig. 1.11. Proposed topology for single-phase to three-phase system

The authors of [71–73] proposed a three-phase to single-phase power conversion system which consists of a power converter, a zero-sequence transformer, and a filter capacitor. The output of the power converter has two stages. The first stage is the

positive sequence, which creates a sinusoidal current in phase with the power supply voltage. This first stage employs a converter to absorb the real, active power and create low harmonic distortion and unity power factor. The second stage consists of the zero-sequence which makes a single-phase voltage for the single-phase load. The active power filter used the power factor correction technique as shown in Fig. 1.12.

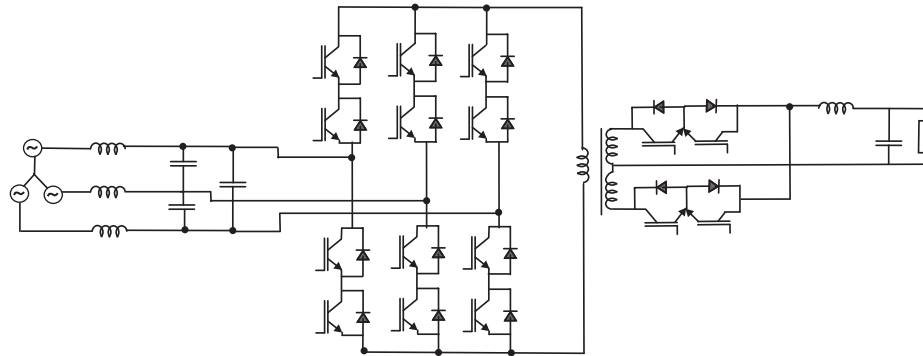


Fig. 1.12. Proposed topology for three-phase to single-phase system

1.2.5 Three-phase Four-wire Power Conversion Systems

Many papers have been presented on various topologies and control methods for three-phase four wire loads. This type of application has three wires feeding current to a three phase load while an extra wire is used as a neutral as shown if Fig 1.13. The authors of [74] proposed a controller based on three single-phase IGBT switches which create a bidirectional converter that can operate under variable load conditions.

A very common problem with three-phase, four wire converters is the current harmonics that appear on the neutral line during unbalanced or varying loads. As a simple solution to current harmonics, the authors of [75] suggested a synchronous machine as a passive method of reducing the harmonics. In [76], an active filter in series connection with the neutral line is used to suppress current harmonics. The authors of [77, 78], presented a shunt active filter to provide compensation currents that balance harmonics and produce unity power factor of the fundamental source

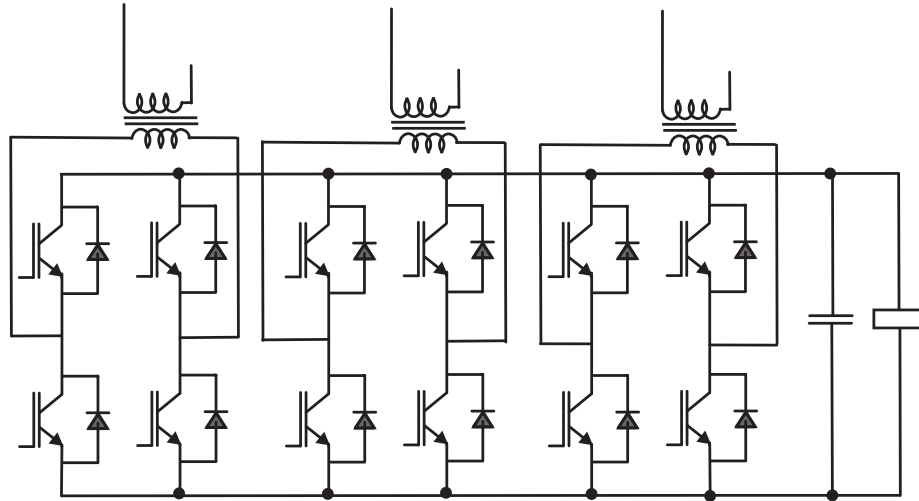


Fig. 1.13. Voltage and frequency controller

current. In [79, 80], the compensation principle and topologies of active power filters for three-phase, four wire systems are explained.

Other papers present active power filters that are more complex. The authors of [81, 82] applied Fast Fourier Transform to choose switching states and to eliminate harmonics on all three phase lines as well as the neutral line. The authors also presented a way to use current-space-vector control of an active power filter to eliminate harmonics on all four lines of the converter. In [83–85], the authors presented a composite control strategy called unified power quality conditioning (UPQC). This strategy can compensate for nonlinear and unbalanced three-phase four wire systems. The strategy reduced harmonic currents and compensates for the reactive power of loads. UPQC can produce source current with a power factor close to unity.

1.3 Objectives

This section presents the main objectives for this research such as:

- Deeply understanding the electrical energy conversion process by using static converters requiring a controlled DC to AC conversion with bidirectional capability.
- Propose the new solution for power electronics conventions with specific advantages as compared to conventional ones.
- Model the converter with the equations to describe the system behavior.
- Develop control and PWM strategies to address the demands of the new converters.
- Simulate the proposed systems to anticipate the behavior of the variables and test the control approach.
- Specify and design of the converter.
- Comparison between proposed and conventional converters.
- Experimental validation of the new systems.

1.4 Thesis Organization & Technical Publications

This section will present the thesis organization and the publications which they accomplished during the research study.

1.4.1 Thesis Organization

This thesis is organized as follows:

- Chapter 2 presents the Single-phase Non-Isolated Bidirectional DC-DC-AC. This chapter bring the new topology for the single-phase converter.
- Chapter 3 discusses about the novel bidirectional DC-DC-AC three-phase power converter. This chapter shows and describes the new method to convert the DC-AC or AC-DC for the three-phase systems.

- Chapter 4 illustrates the DC-DC-AC power converter for three-phase four-wire with bidirectional characteristic. In this chapter the new method allows to have access for the neutral point, in addition the three-phase points are available.
- Chapter 5 presents an experimental result for the single-phase, three-phase and three-phase with four-wire bidirectional power converters to verify that the jobs were completed in the previous chapters.
- Finally the conclusions for this thesis are provided in chapter 6.

1.4.2 Technical Publications

During the development of this research, the author has published three conference papers [86–88], which are related to the single-phase, the three-phase and the three-phase four-wire DC-DC-AC converters, respectively.

2. SINGLE-PHASE NON-ISOLATED BIDIRECTIONAL DC-DC-AC CONVERTER

This chapter compares and proposes non-isolated bidirectional DC-DC-AC converters for applications in single-phase systems, as depicted in Figs. 2.1(a) and 2.1(b), respectively. The main advantages of the proposed converters are reduction of one power switch and high level of integration, while keeping the same features of the conventional solution, such as bidirectional power flow between dc and ac converter sides and independent control in both dc and ac parts by using a unique power conversion circuit. Despite proposing a new solution, this chapter presents a PWM strategy, suitable control approach for the proposed system, as well as simulated result.

2.1 Model of the Converter

The proposed converter is presented in Fig. 2.1(b) . Converter is constituted by a three-switch leg, which is shared by dc and ac converter sides. Such three-switch leg is composed of the power switches q_{1a} , q_{1b} , and q_{1c} . A binary variable is associated with each switch, (i.e., $q_{1x} = 1$ is used when the switch is closed, and $q_{1x} = 0$ when the power switch is open, with $x = a, b, c$). Notice that, as observed in the conventional converter (with two switches per leg), the switches in the three-switch leg cannot be turned on simultaneously, which will avoid a short-circuit through dc-link capacitor. In this way, eight possible switching states could be obtained for this leg, since there

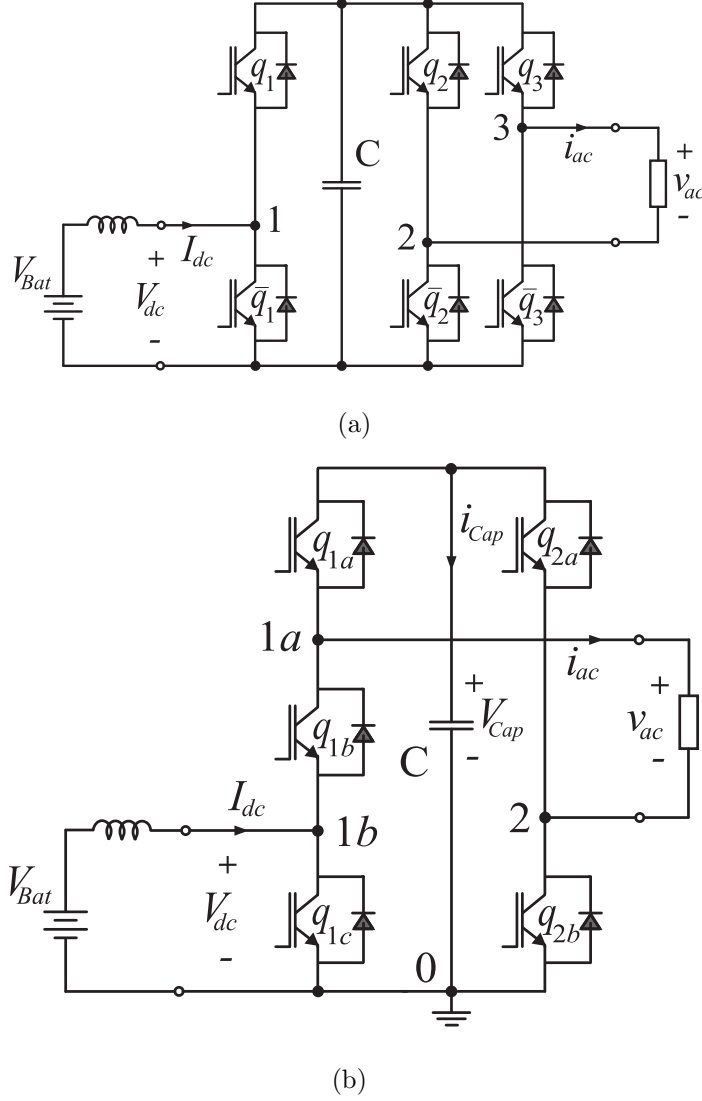


Fig. 2.1. Single-phase non-isolated bidirectional DC-DC-AC converters: (a) conventional and (b) proposed solutions.

are three switches with two switching states each ($q_x = 1$ and $q_x = 0$). Many of these switching states are prohibited, because of either a short-circuit or one of the unwanted switching states. For instance, when is trying to generate lower voltage at point 1a [see Fig. 2.1(b)] than that at point 1b. Table 2.1 shows all possible states with the indication of no-prohibited states, which are highlighted in this table. From Table 2.1 it is possible to write the equations related to the three-leg switch, as

Table 2.1
Indication of prohibited switching states of three-switch leg.

States	q_{1a}	q_{1b}	q_{1c}	Prohibited States
1	0	0	0	Yes
2	0	0	1	Yes
3	0	1	0	Yes
4	0	1	1	No
5	1	0	0	Yes
6	1	0	1	No
7	1	1	0	No
8	1	1	1	Yes

follows:

$$v_{1a0} = [q_{1a} (1 - q_{1b}q_{1c})] V_{Cap} \quad (2.1)$$

$$v_{1b0} = [q_{1a}q_{1b} (1 - q_{1c})] V_{Cap} \quad (2.2)$$

where V_{Cap} is the dc-link voltage.

For the proposed single-phase converter, in order to define the voltages at dc and ac converter sides, it is necessary to write the voltage at the second leg, (i.e., v_{20}), which is given by:

$$v_{20} = q_{2a}V_{Cap} \text{ or } v_{20} = (1 - q_{2b}) V_{Cap} \quad (2.3)$$

where q_{2a} and q_{2b} are the state of the switches of the second leg, with $q_{2y} = 1$ and $q_{2y} = 0$ ($y = a, b$) meaning closed and open switches, respectively. Once the voltages v_{1a0} , v_{1b0} and v_{20} are defined, it is possible to write the voltages at dc and ac converter sides, as follows:

$$V_{dc} = v_{1b0} = [q_{1a}q_{1b} (1 - q_{1c})] V_{Cap} \quad (2.4)$$

$$v_{ac} = v_{1a0} - v_{20} = [q_{1a} (q_{1b} + q_{1c}) - 2q_{1a}q_{1b}q_{1c} - q_{2a}]V_{Cap} \quad (2.5)$$

2.2 PWM Strategy

The voltages generated at the dc and ac converter sides were obtained for the single-phase converter as a function of the state of switches, as in (2.4),(2.5) respectively. The goal of the PWM strategy is to define the state of the switches to guarantee that the desired dc and ac voltages will be generated by the converters. The gating signals of the switches must be obtained to avoid the prohibited states (short-circuit or one of the unwanted switching states) of the proposed converters as well as to guarantee independent control at both converter sides.

If the desired voltages for the dc and ac converter sides are given respectively by V_{dc}^* and $v_{ac}^* = V_{ac}^* \cos(\omega t)$, where V_{ac}^* is the peak value of the reference voltage, then

the reference voltages from the points 1a, 1b and 2 to the point 0 may be expressed as:

$$v_{1b0}^* = V_{dc}^* \quad (2.6)$$

$$v_{1a0}^* = \frac{v_{ac}^*}{2} + V_{offset}^* \quad (2.7)$$

$$v_{20}^* = -\frac{v_{ac}^*}{2} + V_{offset}^* \quad (2.8)$$

where V_{offset}^* is the voltage to avoid the prohibited states, with $V_{offset}^* = V_{dc}^* + V_{ac}^*$. The amplitude modulation ratio can be defined as $m_a = 2V_{ac}^*/(V_{Cap}^* - V_{dc}^*)$.

Once the reference voltages have been determined, the pulse-widths and consequently gating signals are generated with programmable timers. Alternatively, the gating signals can be generated comparing modulating reference signals v_{1a0}^* , v_{1b0}^* and v_{20}^* with a high frequency triangular carrier signal, as observed in Fig. 2.2.

Fig. 2.3 shows the relationship between THD versus the modulation ratio (m_a). As expected, as far as m_a increases the THD is reduced.

2.3 Control Strategy

Fig. 2.4 presents the converter control block diagram. The capacitor voltage V_{Cap} is adjusted to its reference V_{Cap}^* value by using a controller PI_v . This controller provides the amplitude of the reference current I_{dc}^* . The current controller is implemented by using a controller indicated by the block PI_i , which furnishes the voltage V_{dc}^* employed in the PWM scheme presented in Section 2.2. The ac voltages for the single-phase converters have been obtained in open-loop (v_{ac}^*). V_{Bat} in Fig. 2.4 is considered as a disturbance for the controller. It is assumed that the current controller will be able to compensate this term. One way to define the gains of the proportional-integrator (PI) controller is writing the open-loop ($H(s)$) and closed-loop ($G(s)$) transfer functions. The open loop transfer function is given by:

$$H(s) = \frac{K_i(\frac{K_p}{K_i}s + 1)}{s} \frac{\frac{1}{R}}{\frac{L}{R}s + 1} \quad (2.9)$$

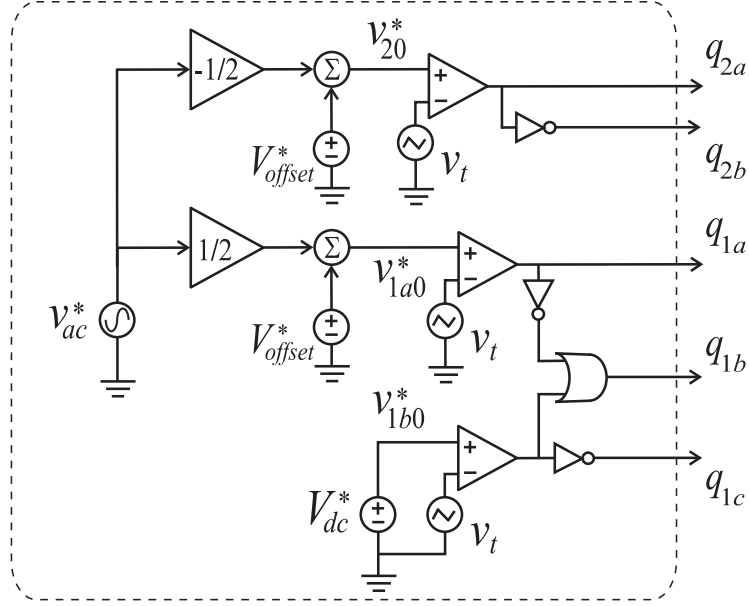


Fig. 2.2. PWM strategy: single-phase converter.

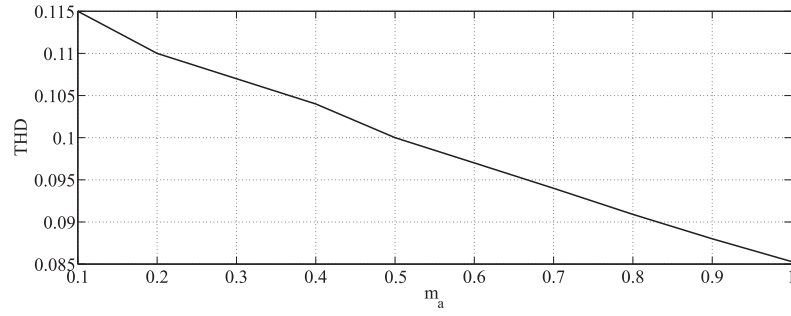


Fig. 2.3. THD of the output current as a function of m_a .

Canceling the zero of the controller with the pole of the system, the open loop transfer function depends only of the K_i and R as follows:

$$H(s) = \frac{K_i}{Rs} \quad (2.10)$$

And

$$\frac{K_i}{K_p} = \frac{R}{L} \quad (2.11)$$

The closed-loop transfer function is obtained as below:

$$G(s) = \frac{K_i}{K_i + Rs} \quad (2.12)$$

Which means a pole placed at:

$$s = -\frac{K_i}{R} \quad (2.13)$$

Equations (2.11) and (2.13) are enough to find the controller's gains. The design of the gains of the voltage controller can be obtained similarly.

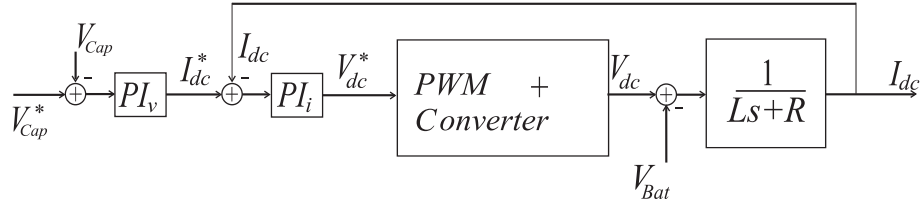


Fig. 2.4. Control block diagram.

2.4 Dc-link Capacitor Variables

The dc-link capacitor current (i_{Cap}) for single-phase conventional and proposed converter can be written respectively as follows:

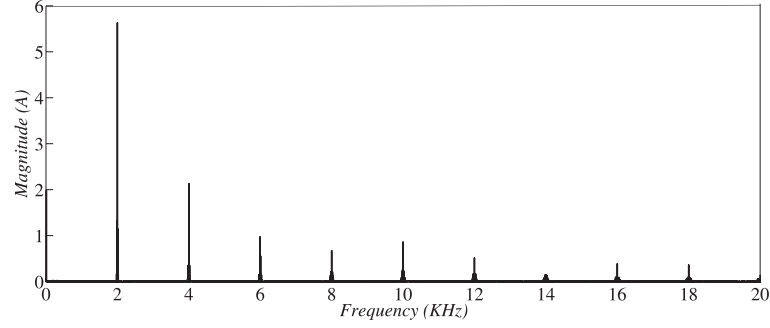
$$i_{Cap} = q_1 I_{dc} - q_2 i_{ac} - q_3 i_{ac} \quad (2.14)$$

$$i_{Cap} = q_{1a}(q_{1b} I_{dc} - i_{ac}) - q_{2a} i_{ac} \quad (2.15)$$

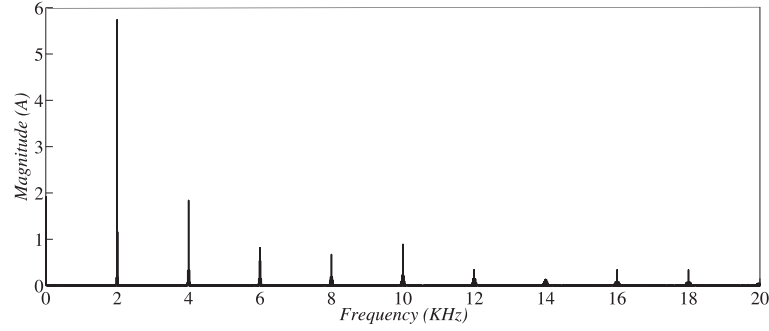
Alternatively, the dc-link capacitor currents for the conventional and proposed converters can be obtained as a function of input and output powers as presented below:

$$i_{Cap} = \frac{P_{in}}{V_{cap}} - \frac{P_{out}}{V_{cap}} \quad (2.16)$$

$$i_{Cap} = \frac{P_{in}}{V_{cap}} \left(\frac{v_{1a0}^*}{V_{cap}} \right) - \frac{P_{out}}{V_{cap}} \quad (2.17)$$



(a)



(b)

Fig. 2.5. dc-link capacitor current versus frequency using triangular:
(a) Conventional topology (b) Proposed topology

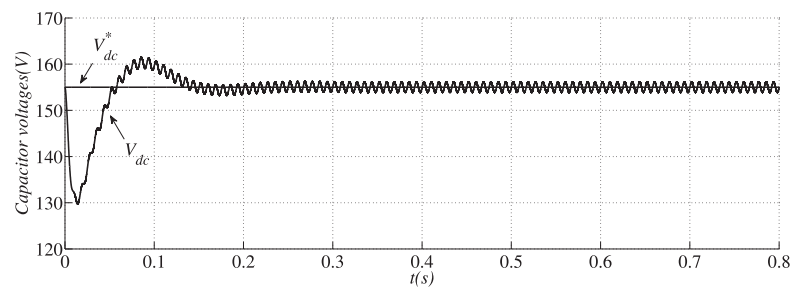
Fig. 2.5 illustrates the harmonic spectrum of the dc-link capacitor current. In this case, the proposed topology provides the reduction of the high-order harmonic frequencies when compared with conventional one. Due to the three-switch leg, which requires a V_{offset} (to avoid the prohibited states), the dc-link capacitor voltage for the proposed converters is larger than that of the conventional ones. In this case dc-link capacitor voltage is defined by the sum of ac and dc desired voltages. But the lost is almost the same in both conventional and proposed converters.

2.5 Simulated Results

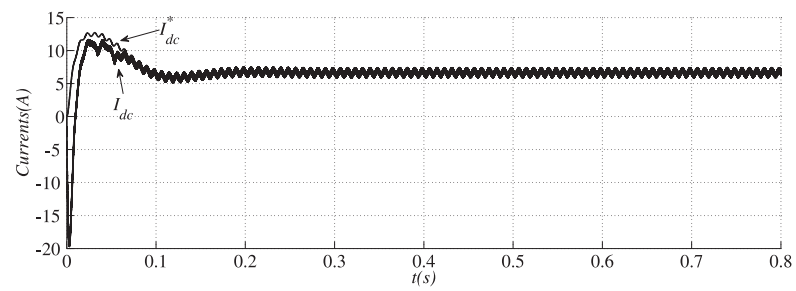
The proposed and conventional single-phase converters have been tested throughout dynamic simulation with PSIM software. The modulation strategy has been performed in C language by using DLL block. The simulation results were obtained with the following parameters: $V_{dc} = 45V$; $f_s = 20KHz$.

Fig. 2.6, Fig. 2.7 show the simulation results for the single-phase conventional converter and Fig. 2.8, Fig. 2.9 show the simulation result for the proposed converter. Fig. 2.6(a) and Fig. 2.8(a) are showing the reference ($V_{Cap}^* = 155V$) and measured (V_{Cap}) capacitor voltages, 2.6(b) and 2.8(b) are showing the reference current and measured current in the dc side while Figs. 2.7(a), 2.7(b), Figs. 2.9(a) and 2.9(b) depict respectively the ac voltage (v_{ac}) and current (i_{ac}). The line-line voltage has 3 levels, due to, the pole voltages at point 1a and 2 are V_{dc} or 0 as depicted in Fig. 2.9(a).

As it shown in Figs. 2.8(a)-(b), the transient mode is less than 0.1s and the current and the voltage reach the steady state too fast and the error of the steady state is zero.

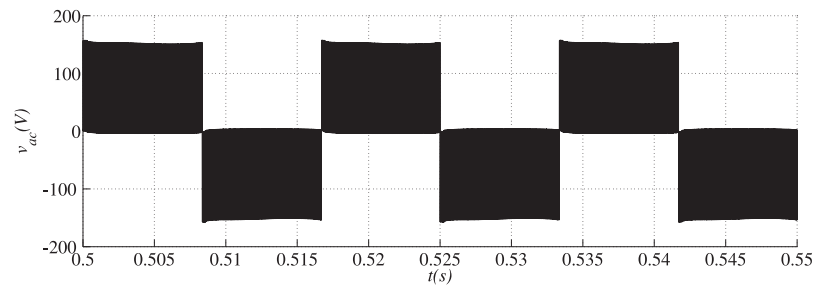


(a)

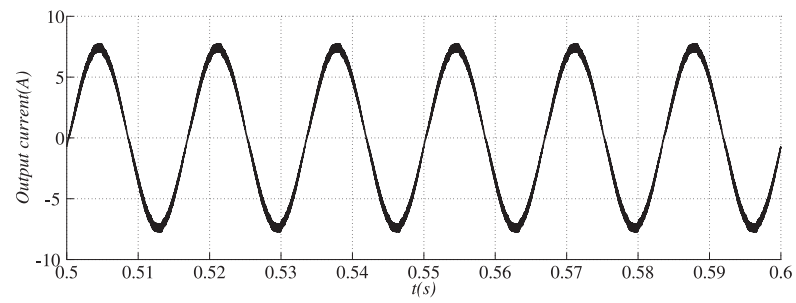


(b)

Fig. 2.6. Simulation results for the single-phase converter: (a) reference and measured capacitor voltages, and (b) reference and measured dc currents.

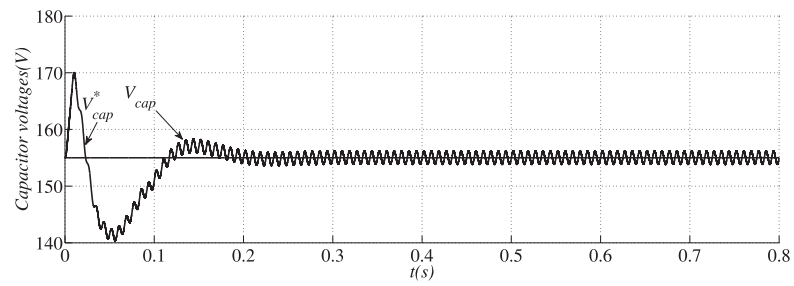


(a)

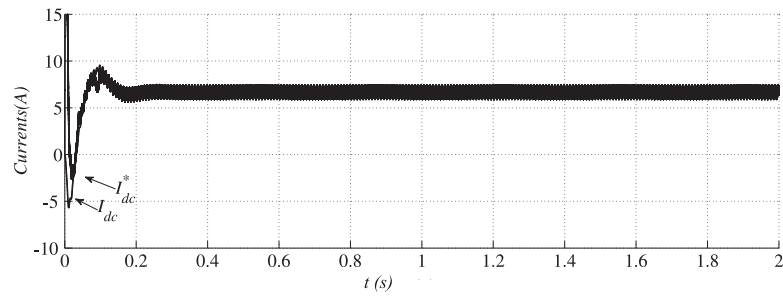


(b)

Fig. 2.7. Simulation results for the single-phase converter: (a) voltage at ac converter side, and (b) current at ac converter side.

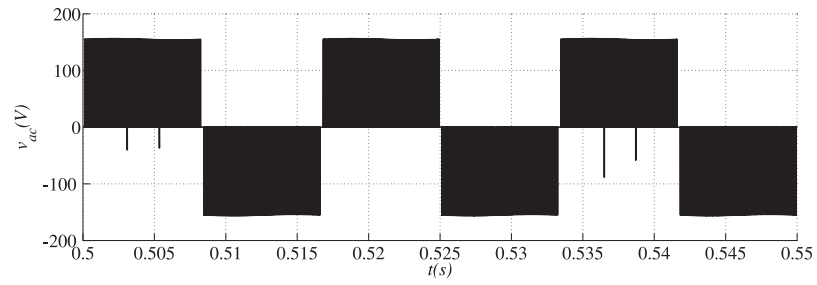


(a)

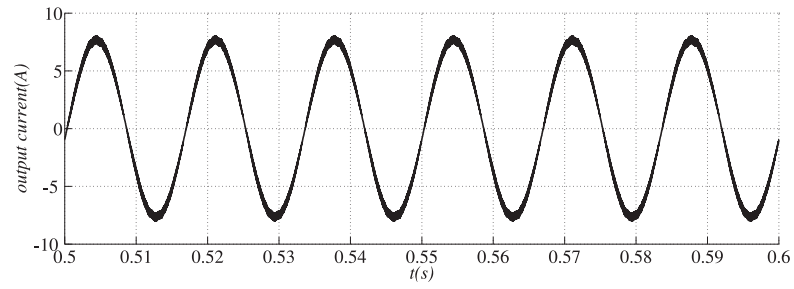


(b)

Fig. 2.8. Simulation results for the single-phase converter: (a) reference and measured capacitor voltages, and (b) reference and measured dc currents.



(a)



(b)

Fig. 2.9. Simulation results for the single-phase converter: (a) voltage at ac converter side, and (b) current at ac converter side.

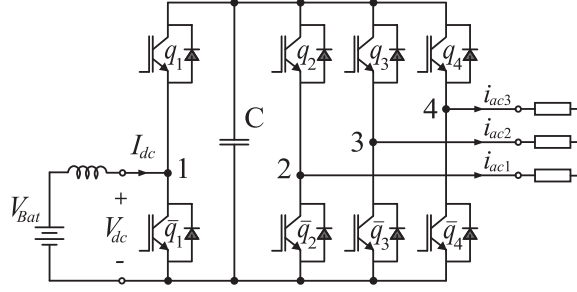
3. BIDIRECTIONAL DC-DC-AC THREE-PHASE POWER CONVERTER

This chapter compares and proposes a DC-DC-AC converters for applications in three-phase systems, as depicted in Figs. 3.1(a) and 3.1(b), respectively. The main advantages of the proposed converter are reduction of one power switch and high level of integration, while keeping the same features of the conventional solution, such as (i) bidirectional power flow between dc and ac micro-grids, (ii) independent control in both dc and ac parts, and (iii) different operation conditions using a unique power conversion circuit. Despite proposing a new solution, this chapter presents an optimized PWM strategy, as well as a suitable control approach for the proposed system, as well as simulated result.

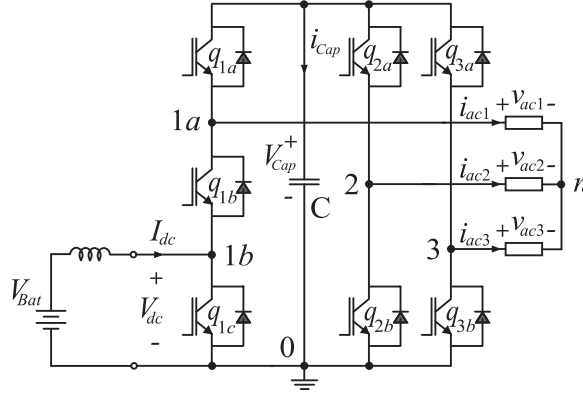
3.1 Model of the Converter

The proposed converters are presented in Fig. 3.1(b). This converter is constituted by a three-switch leg, which is shared by dc and ac converter sides. Such three-switch leg is composed of the power switches q_{1a} , q_{1b} , and q_{1c} . A binary variable is associated with each switch, (i.e., $q_{1x} = 1$ is used when the switch is closed, and $q_{1x} = 0$ when the power switch is open, with $x = a, b, c$). Notice that, as observed in the conventional converter (with two switches per leg), the switches in the three-switch leg cannot be turned on simultaneously, which will avoid a short-circuit through dc-link capacitor.

In this way, eight possible switching states could be obtained for this leg, since there are three switches with two switching states each ($q_x = 1$ and $q_x = 0$). Many of these switching states are prohibited, because of either a short-circuit or one of the unwanted switching states. For instance, when is trying to generate lower voltage at



(a)



(b)

Fig. 3.1. Bidirectional converter interfacing DG system, hybrid dc and ac micro-grid: (a) conventional solution with eight switches, (b) proposed solution with seven switches and .

point 1a [see Fig. 3.1(b)] than that at point 1b. Table 3.1 shows all possible states with the indication of no-prohibited states, which are highlighted in this table.

From Table 3.1 it is possible to write the equations related to the three-leg switch, as follows:

$$v_{1a0} = [q_{1a}(1 - q_{1b}q_{1c})] V_{Cap} \quad (3.1)$$

$$v_{1b0} = [q_{1a}q_{1b}(1 - q_{1c})] V_{Cap} \quad (3.2)$$

Table 3.1
Indication of prohibited switching states of three-switch leg.

States	q_{1a}	q_{1b}	q_{1c}	Prohibited States
1	0	0	0	Yes
2	0	0	1	Yes
3	0	1	0	Yes
4	0	1	1	No
5	1	0	0	Yes
6	1	0	1	No
7	1	1	0	No
8	1	1	1	Yes

where V_{Cap} is the dc-link voltage. For the proposed three-phase converter, in order to define the voltages at dc and ac converter sides, it is necessary to write the voltage at the third leg, (i.e., v_{20} and v_{30}), which is given by:

$$v_{20} = q_{2a}V_{Cap} \text{ or } v_{20} = (1 - q_{2b})V_{Cap} \quad (3.3)$$

$$v_{30} = q_{3a}V_{Cap} \text{ or } v_{30} = (1 - q_{3b})V_{Cap} \quad (3.4)$$

where q_{3a} and q_{3b} are the state of the switches of the third leg, with $q_{3y} = 1$ and $q_{3y} = 0$ ($y = a, b$) meaning closed and open switches, respectively.

Once the voltages v_{1a0} , v_{1b0} , v_{20} and v_{30} are defined, it is possible to write the voltages at dc and ac converter sides, i.e.:

$$V_{dc} = v_{1b0} = [q_{1a}q_{1b}(1 - q_{1c})]V_{Cap} \quad (3.5)$$

$$v_{ac1} = v_{1a0} - v_{n0} = [q_{1a}(q_{1b} + q_{1c}) - 2q_{1a}q_{1b}q_{1c}]V_{Cap} - v_{n0} \quad (3.6)$$

$$v_{ac2} = v_{20} - v_{n0} = q_{2a}V_{Cap} - v_{n0} \quad (3.7)$$

$$v_{ac3} = v_{30} - v_{n0} = q_{3a}V_{Cap} - v_{n0} \quad (3.8)$$

where v_{n0} is the voltage of point n referred to the 0, which is given by $v_{n0} = \frac{1}{3}[q_{1a}(1 - q_{1b}q_{1c}) + 2 - q_{2a} - q_{3a}]V_{Cap}$.

3.2 PWM Strategy

The voltages generated at the dc and ac converter sides were obtained for the three-phase converters as a function of the state of switches, as in (3.5)-(3.8). The goal of the PWM strategy is to define the state of the switches to guarantee that the desired dc and ac voltages will be generated by the converters. The gating signals of the switches must be obtained to avoid the prohibited states (short-circuit or one of the unwanted switching states) of the proposed converters as well as to guarantee independent control at converter sides. If the desired voltages for the dc and ac converter sides

are given respectively by V_{dc}^* and $v_{ac1}^* = V_{ac}^* \cos(\omega t)$, $v_{ac2}^* = V_{ac}^* \cos(\omega t + 120^\circ)$ and $v_{ac3}^* = V_{ac}^* \cos(\omega t + 240^\circ)$, then the reference voltages from the points 1a, 1b, 2 and 3 to the point 0 may be expressed as:

$$v_{1b0}^* = V_{dc}^* \quad (3.9)$$

$$v_{1a0}^* = v_{ac1}^* + V_{offset}^* + v_\mu^* \quad (3.10)$$

$$v_{20}^* = v_{ac2}^* + V_{offset}^* + v_\mu^* \quad (3.11)$$

$$v_{30}^* = v_{ac3}^* + V_{offset}^* + v_\mu^* \quad (3.12)$$

where V_{offset}^* is the voltage to avoid the prohibited states given by $V_{offset}^* = V_{dc}^* + V_{ac}^*$, and v_μ^* is the voltage that can be calculated by taking into account the apportioning factor μ . v_μ^* is derived by using the same approach employed in the three-phase PWM modulator [89], [90], and presented below:

$$v_\mu^* = E\left(\mu - \frac{1}{2}\right) - \mu v_{\max}^* + (\mu - 1)v_{\min}^* \quad (3.13)$$

where $v_{\max}^* = \max V$ and $v_{\min}^* = \min V$ and where,

$$V = \{v_{ac1}^* + V_{offset}^*, v_{ac2}^* + V_{offset}^*, v_{ac3}^* + V_{offset}^*\}.$$

The apportioning factor μ ($0 \leq \mu \leq 1$) is given by

$$\mu = t_{oi}/t_o \quad (3.14)$$

and indicates the distribution of the general free-wheeling period t_o (period in which voltages v_{1a0} , v_{20} and v_{30} are equal) at the beginning ($t_{oi} = \mu t_o$) and at the end ($t_{of} = (1 - \mu)t_o$) of the switching period T [89], [90]. The apportioning factor can be obtained to reduce the Total Harmonic Distortion (THD) of the ac converter voltages.

In this case, the proposed algorithm is: Step 1. Choose the general apportioning factor μ and calculate v_μ^* from (3.13).

Step 2. Determine v_{1a0}^* , v_{20}^* and v_{30}^* from (3.10)-(3.12).

Step 3. Once the reference voltages have been determined, the pulse-widths and consequently the gating signals are generated with programmable timers.

$$\tau_j = \left(\frac{v_j^*}{V_{cap}}\right)T \quad (j = 1a0, 20, 30) \quad (3.15)$$

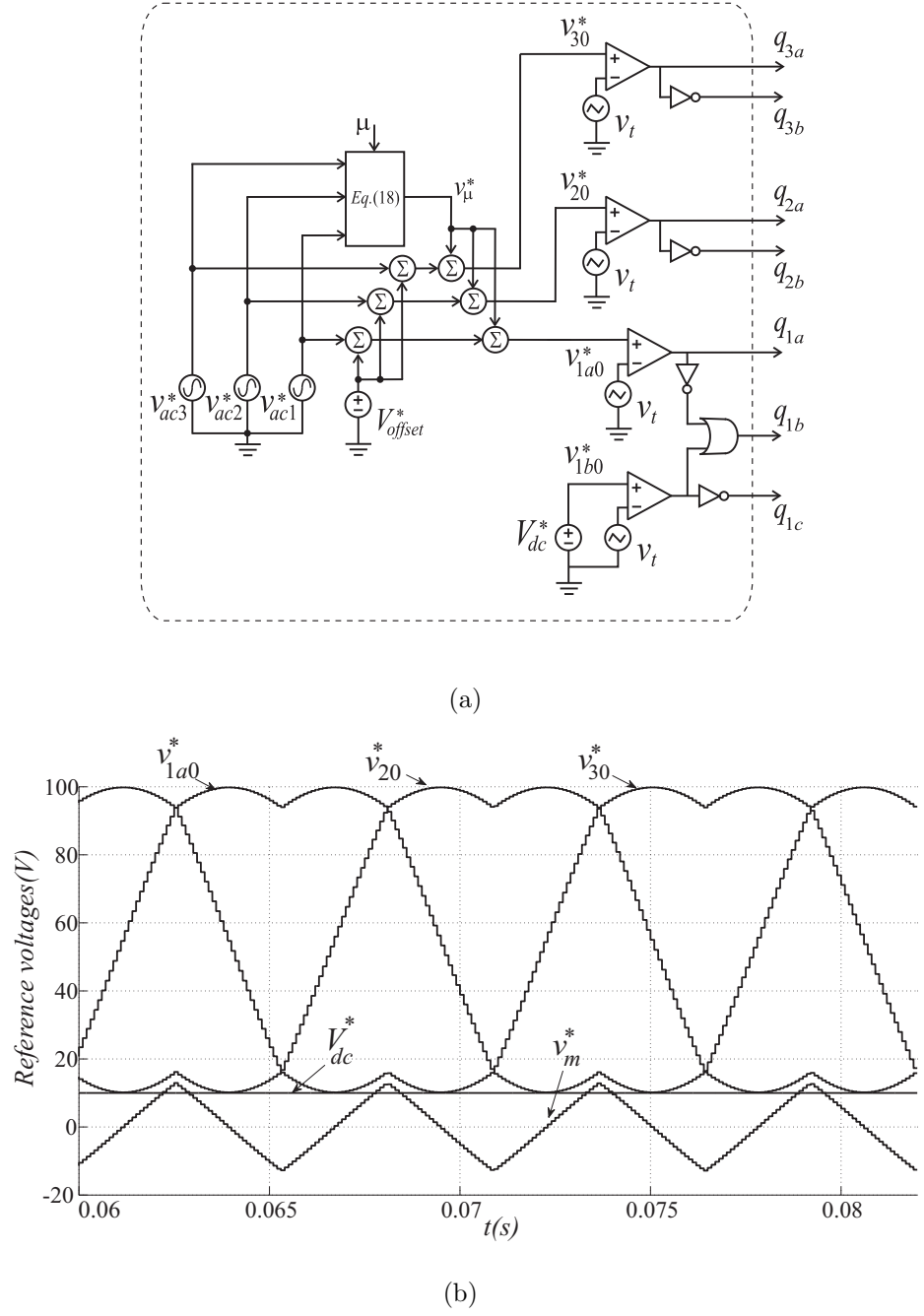


Fig. 3.2. (a) PWM strategy, and (b) reference voltage: v_{1i0}^* , v_{1o0}^* , v_{2o0}^* , v_{3o0}^* , v_{μ}^* , and V_{dc}^* .

Alternatively, the gating signals can be generated comparing modulating reference signals v_{1a0}^* , v_{1b0}^* , v_{20}^* and v_{30}^* with a high frequency triangular carrier signal, as depicted in Fig. 3.2(a).

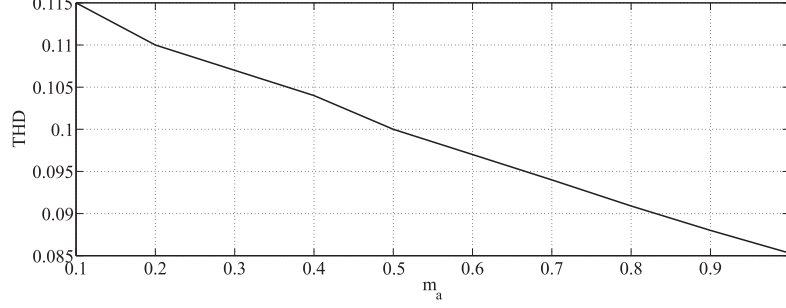


Fig. 3.3. THD of the output current as a function of m_a .

Fig. 3.2(b) shows the reference voltage v_{1a0}^* , v_{20}^* , v_{30}^* , v_{μ}^* , and V_{dc}^* for $m_a=1.0$ and $\mu = 0.5$, while Fig. 3.3 shows the relationship between THD versus the modulation ratio (m_a). As expected, as far as m_a increases the THD is reduced.

3.3 Control Strategy

Fig. 3.4 presents the converter control block diagram. The capacitor voltage V_{Cap} is adjusted to its reference V_{Cap}^* value by using a controller PI_v . This controller provides the amplitude of the reference current I_{dc}^* . The current controller is implemented by using a controller indicated by the block PI_i , which furnishes the voltage V_{dc}^* employed in the PWM scheme presented in Section 3.2. The ac voltages for the three-phase converters have been obtained in open-loop (v_{ac1}^* , v_{ac2}^* and v_{ac3}^*). V_{Bat} in Fig. 3.4 is considered as a disturbance for the controller. It is assumed that the current controller will be able to compensate this term. One way to define the gains of the proportional-integrator (PI) controller is writing the open-loop ($H(s)$) and closed-loop ($G(s)$) transfer functions. The open loop transfer function is given by:

$$H(s) = \frac{K_i(\frac{K_p}{K_i}s + 1)}{s} \frac{\frac{1}{R}}{\frac{L}{R}s + 1} \quad (3.16)$$

Canceling the zero of the controller with the pole of the system, the open loop transfer function depends only of the K_i and R as follows:

$$H(s) = \frac{K_i}{Rs} \quad (3.17)$$

And

$$\frac{K_i}{K_p} = \frac{R}{L} \quad (3.18)$$

The closed-loop transfer function is obtained as below:

$$G(s) = \frac{K_i}{K_i + Rs} \quad (3.19)$$

Which means a pole placed at:

$$s = -\frac{K_i}{R} \quad (3.20)$$

Equations (3.18) and (3.20) are enough to find the controller's gains. The design of the gains of the voltage controller can be obtained similarly.

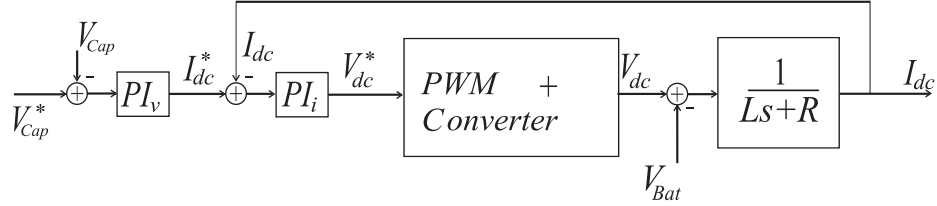


Fig. 3.4. Control block diagram.

3.4 Dc-link Capacitor Variables

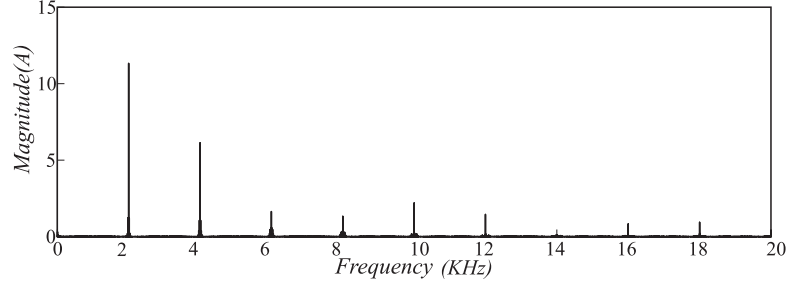
The dc-link capacitor current (i_{Cap}) for the conventional and proposed converters can be written respectively as following:

$$i_{Cap} = q_1 I_{dc} - q_2 i_{ac1} - q_3 i_{ac2} - q_4 i_{ac3} \quad (3.21)$$

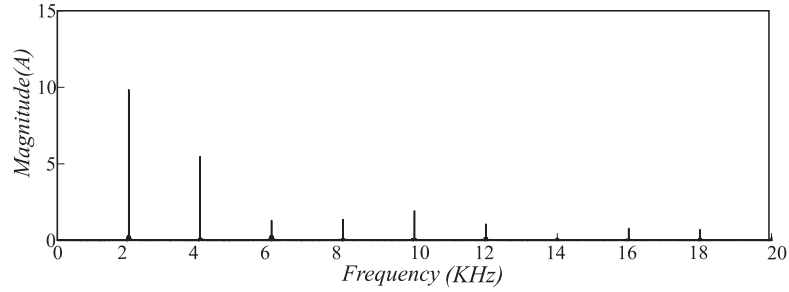
$$i_{Cap} = q_{1a}(q_{1b} I_{dc} - i_{ac1}) - q_{2a} i_{ac2} - q_{3a} i_{ac3} \quad (3.22)$$

Alternatively, the dc-link capacitor currents for the conventional and proposed converters can be obtained as a function of input and output powers as presented below:

$$i_{Cap} = \frac{P_{in}}{V_{cap}} - \frac{P_{out}}{V_{cap}} \quad (3.23)$$



(a)



(b)

Fig. 3.5. dc-link capacitor current versus frequency using triangular:
(a) Conventional topology (b) Proposed topology

$$i_{Cap} = \frac{P_{in}}{V_{cap}} \left(\frac{v_{1a0}^*}{V_{cap}} \right) - \frac{P_{out}}{V_{cap}} \quad (3.24)$$

The power losses on the dc-link capacitor can be calculated by:

$$P_{loss}^{Ho} = 0.45 ESR_{(100Hz)} (I_{c,rms}^{Ho})^2 \quad (3.25)$$

where $ESR_{(100Hz)}$ is the equivalent series resistance at the frequency of 100Hz, and $I_{c,rms}^{Ho}$ is the high-order root mean square (RMS) of the current on the dc-link for high harmonic component ($h > 50$). As ERS is almost constant for frequency higher than 3KHz, the P_{loss}^{Ho} depends only of the $I_{c,rms}^{Ho}$, which means that the reduction of the power losses on the dc-link capacitor is determined by RMS current.

Fig. 3.5 illustrates the harmonic spectrum of the dc-link capacitor current. Comparing (3.23) with (3.24) the term v_{1a0}^*/V_{cap} for the proposed topology will be responsible for the reduction of high frequency components. The proposed topology

provides the reduction of the high-order harmonic frequencies when compared with conventional one and consequently the power losses on the capacitor will be lesser.

The dc-link capacitor voltage for the proposed converter is larger than that of the conventional one due to the three-switch leg, which requires a V_{offset} (to avoid the prohibited states). In this case dc-link capacitor voltage is defined by the sum of ac and dc desired voltages.

3.5 Simulated Results

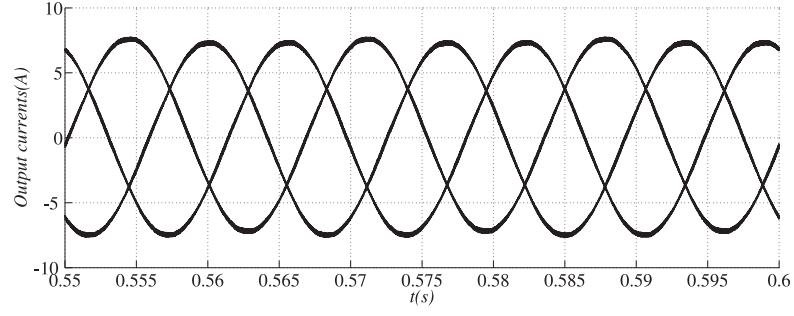
The proposed and conventional three-phase converters have been tested throughout dynamic simulation with PSIM software. The modulation strategy has been performed in C language by using DLL block. The simulation results were obtained with the following parameters: $V_{dc} = 45V$; $f_s = 20KHz$.

Figs. 3.6(a), 3.7, 3.8 and 3.11 show the simulation results for the three-phase conventional converter.

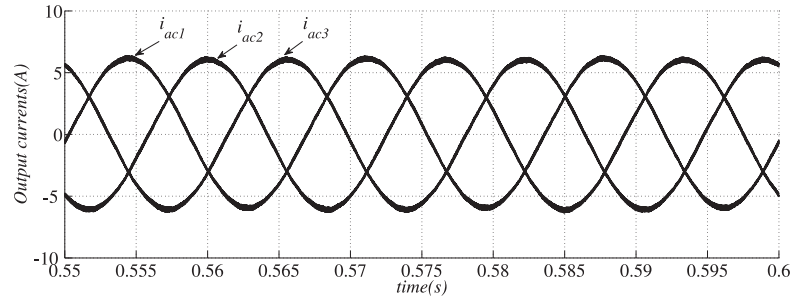
On the other hand, Figs. 3.6(b), 3.9, 3.10, 3.12 and 3.13 show the simulation results for the three-phase proposed one.

Figs. 3.6(a-b) show the three-phase currents (i_{ac1} , i_{ac2} and i_{ac3}) for the conventional converter and the proposed one. Figs. 3.7(a)-(c) and Figs. 3.9(a)-(c) illustrate the behavior of the phase voltages (v_{ac1} , v_{ac2} and v_{ac3}) for the conventional and proposed converters. According to the equations (3.5)-(3.8) in section 3.1, phase voltage for each line has 5 levels.

Figs. 3.8(a)-(c) and Figs. 3.10(a)-(c) show the line-line voltages ($v_{ac12} = v_{ac1} - v_{ac2}$, $v_{ac13} = v_{ac1} - v_{ac3}$ and $v_{ac23} = v_{ac2} - v_{ac3}$) for the conventional converter and the proposed one. From the equations (3.1)-(3.4) in section 3.1, it is possible to see the voltages at points 1a, 2 and 3 [see Fig. 3.1(b)] are V_{dc} or 0. From these two voltages, at the line-line voltages, the possible voltages are V_{dc} , 0 and $-V_{dc}$ as they cause the three level voltages in Figs. 3.10(a)-(c).



(a)



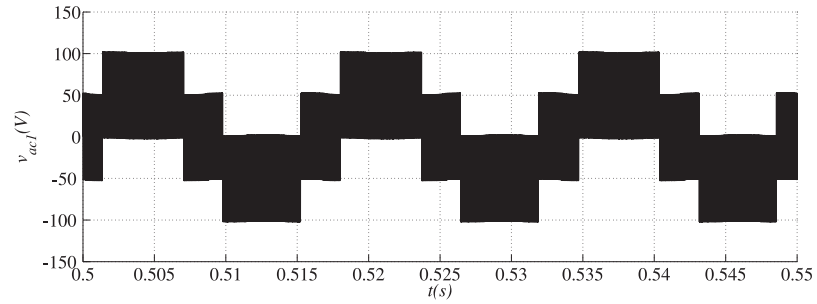
(b)

Fig. 3.6. Three phase currents : (a) conventional topology, (b) proposed topology.

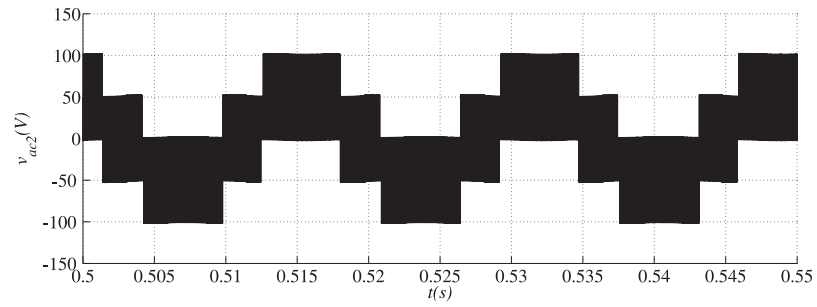
Fig. 3.11 (a) and Fig. 3.12 (a) show the reference ($V_{Cap}^*=155V$) and measured (V_{Cap}) capacitor voltages for the conventional and proposed converters. They have transient mode less than 0.1s which means the controller is too fast and the steady state is 0.

Fig. 3.11(b) shows the reference and measured dc currents for the conventional converter (I_{dc}^* and I_{dc}), on the other hand Fig. 3.12(b) shows the reference and measured dc currents for the proposed converter (I_{dc}^* and I_{dc}), which, both of the converters have the transient mode less than 0.1s and the steady state errors are 0.

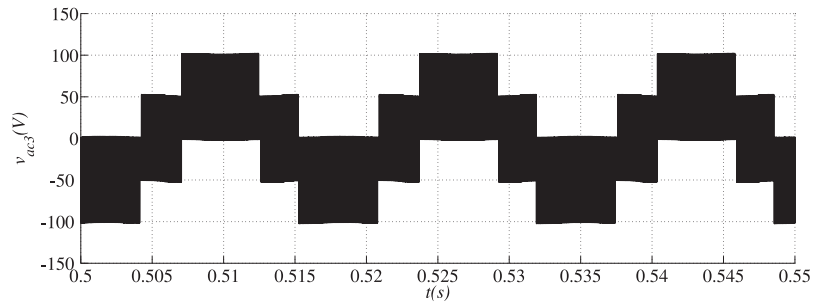
Fig. 3.13(a) the transient operation for the reference and measured currents and Fig. 3.13(b) shows the transient operation for the reference and measured capacitor voltages, which they show, after $t=1$ while the load is being doubled, controllers work properly and the steady state errors become 0.



(a)

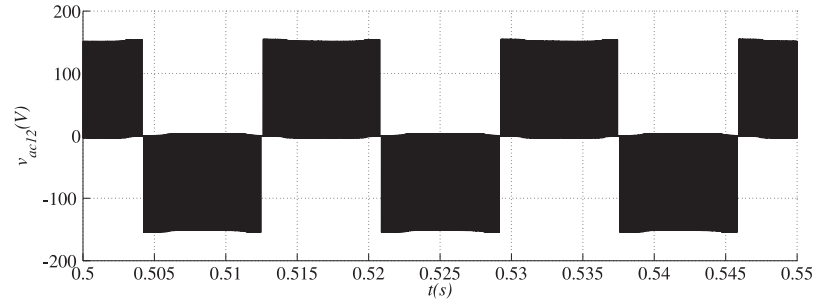


(b)

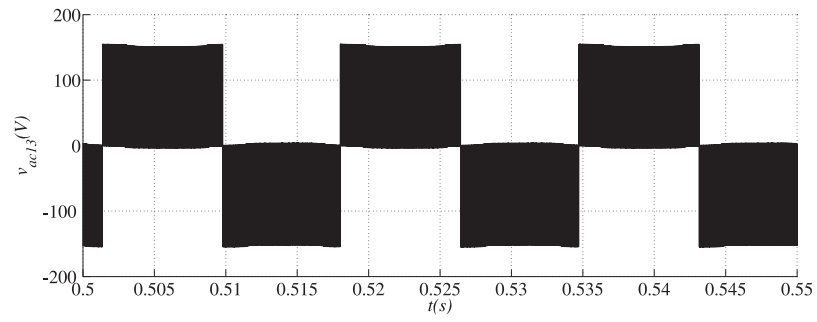


(c)

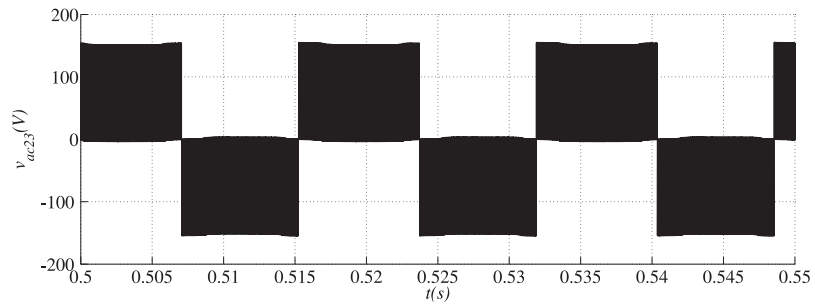
Fig. 3.7. Simulation results for the three-phase conventional converter:(a) phase voltage at phase 1, (b) phase voltage at phase 2, and (c) phase voltage at phase 3.



(a)

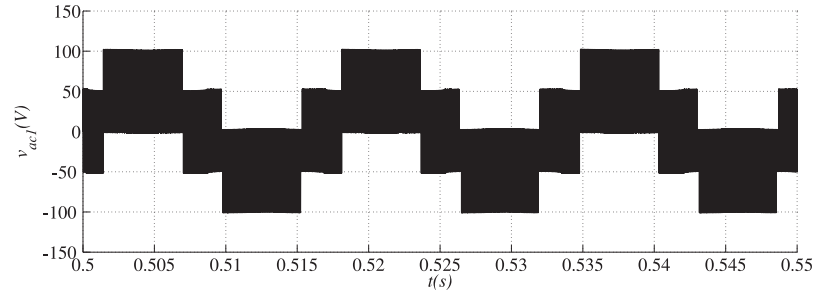


(b)

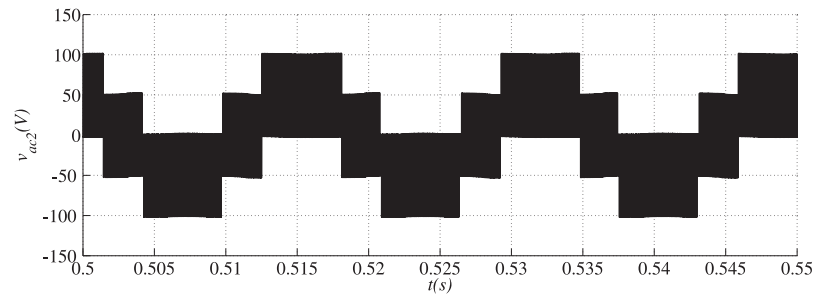


(c)

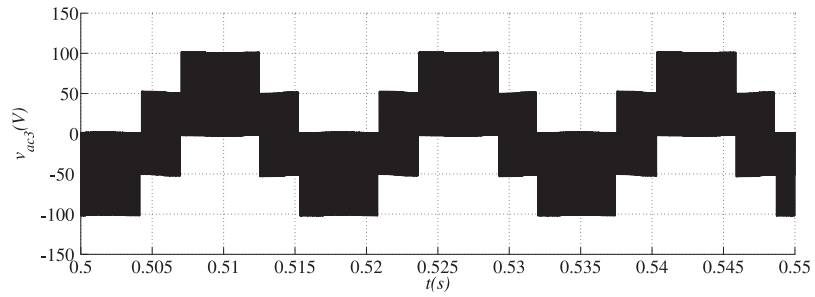
Fig. 3.8. Simulation results for the three-phase conventional converter: (a) line-line voltage (phase 1-2), (b) line-line voltage (phase 1-3), and (c) line-line voltage (phase 2-3).



(a)

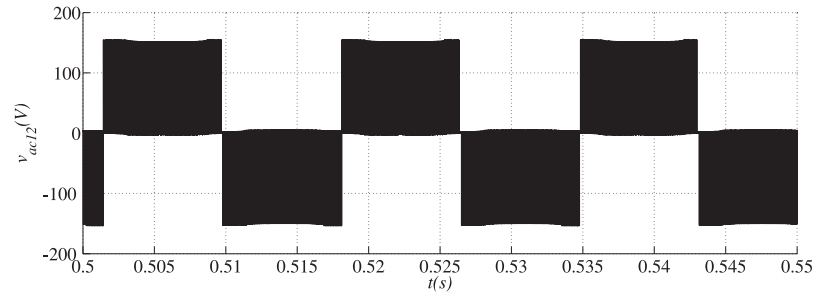


(b)

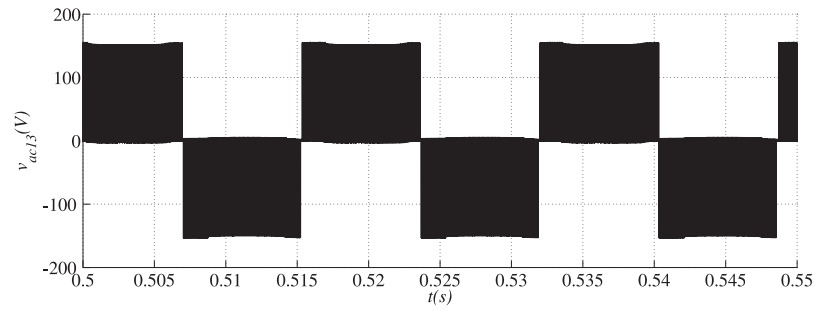


(c)

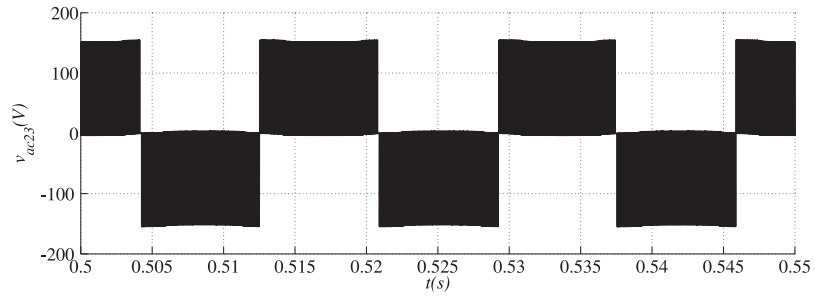
Fig. 3.9. Simulation results for the three-phase proposed converter: (a) phase voltage at phase 1, (b) phase voltage at phase 2, and (c) phase voltage at phase 3.



(a)

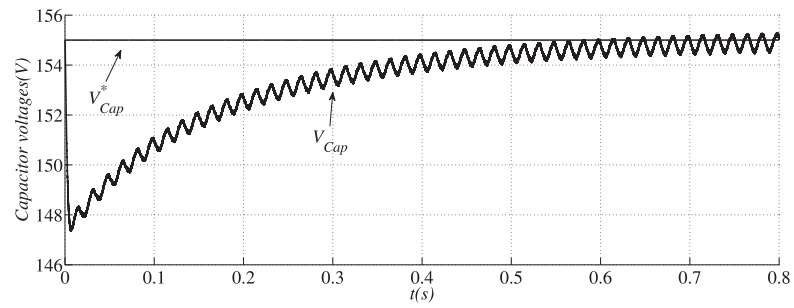


(b)

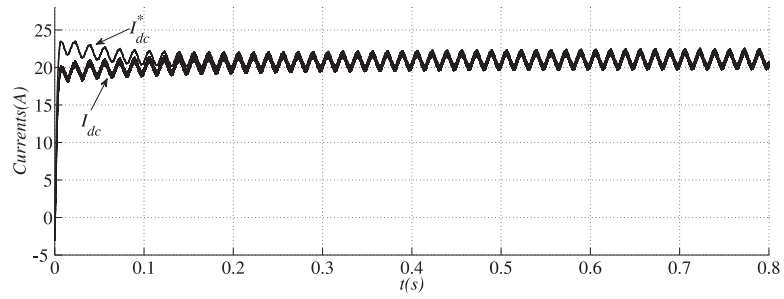


(c)

Fig. 3.10. Simulation results for the three-phase proposed converter: (a) line-line voltage (phase 1-2), (b) line-line voltage (phase 1-3), and (c) line-line voltage (phase 2-3).

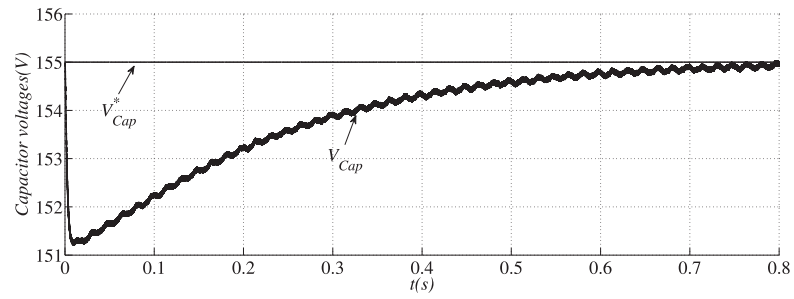


(a)

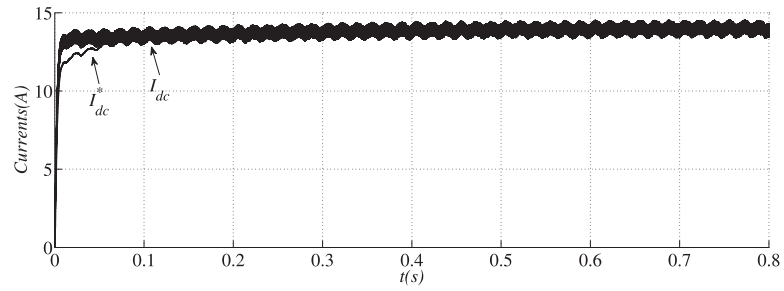


(b)

Fig. 3.11. Simulation results for the three-phase conventional converter: (a) reference and measured capacitor voltages, and (b) reference and measured dc currents.

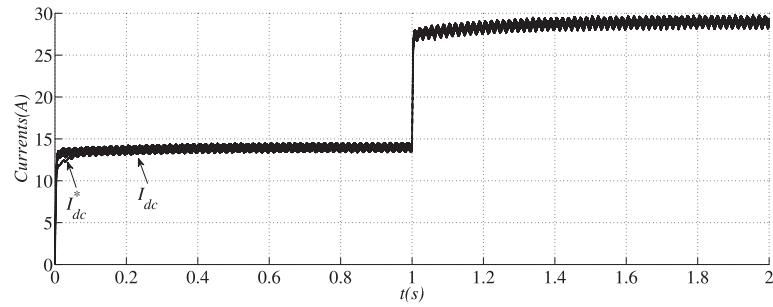


(a)

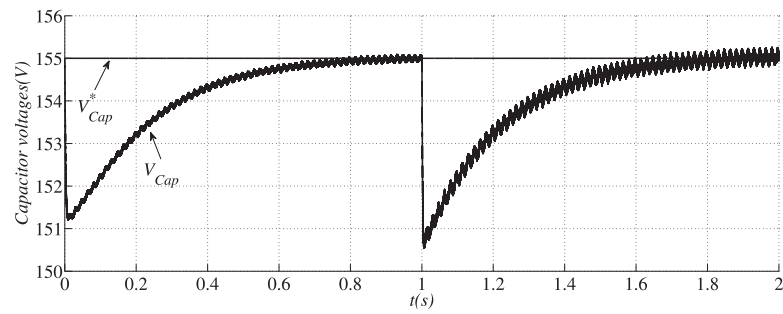


(b)

Fig. 3.12. Simulation results for the three-phase proposed converter: (a) reference and measured capacitor voltages, and (b) reference and measured dc currents .



(a)



(b)

Fig. 3.13. Simulation results for the three-phase converter: (a) transient operation for the reference and measured currents , (b) transient operation for the reference and measured capacitor voltages .

4. DC-DC-AC POWER CONVERTER FOR THREE-PHASE FOUR-WIRE WITH BIDIRECTIONAL CHARACTERISTICS

This chapter proposes a DC-DC-AC three-phase four-wire converter, as depicted in Fig. 4.1(b). The main advantages of the proposed converter are reduction of one power switch and high level of integration, while keeping the same features of the conventional solution, such as (i) bidirectional power flow between dc and ac sides, (ii) independent control in both dc and ac parts, and (iii) ability to handle different operation conditions using a unique power conversion circuit. Despite proposing a new solution, this chapter presents an optimized PWM strategy, as well as a suitable control approach for the proposed system.

4.1 Model of the Converter

The proposed converter is presented in Fig. 4.1(b), which is constituted by four legs, three conventional ones with two switches per leg and one with three switches which is shared by dc and ac converter sides. Such a three-switch leg is composed of the power switches q_{1a} , q_{1b} , and q_{1c} . A binary variable is associated with each switch, (i.e., $q_{1x} = 1$ is used when the switch is closed, and $q_{1x} = 0$ when the power switch is open, with $x = a, b, c$). Notice that, as observed in the conventional converter (with two switches per leg), the switches in the three-switch leg cannot be turned on simultaneously, which will avoid a short-circuit through the dc-link capacitor. In this way, three possible switching states could be obtained for this leg, since there are three switches with two switching states each ($q_x = 1$ and $q_x = 0$). Many of these switching states are prohibited, because of either a short-circuit (as mentioned earlier) or one of the unwanted switching states. For instance, when trying to generate lower

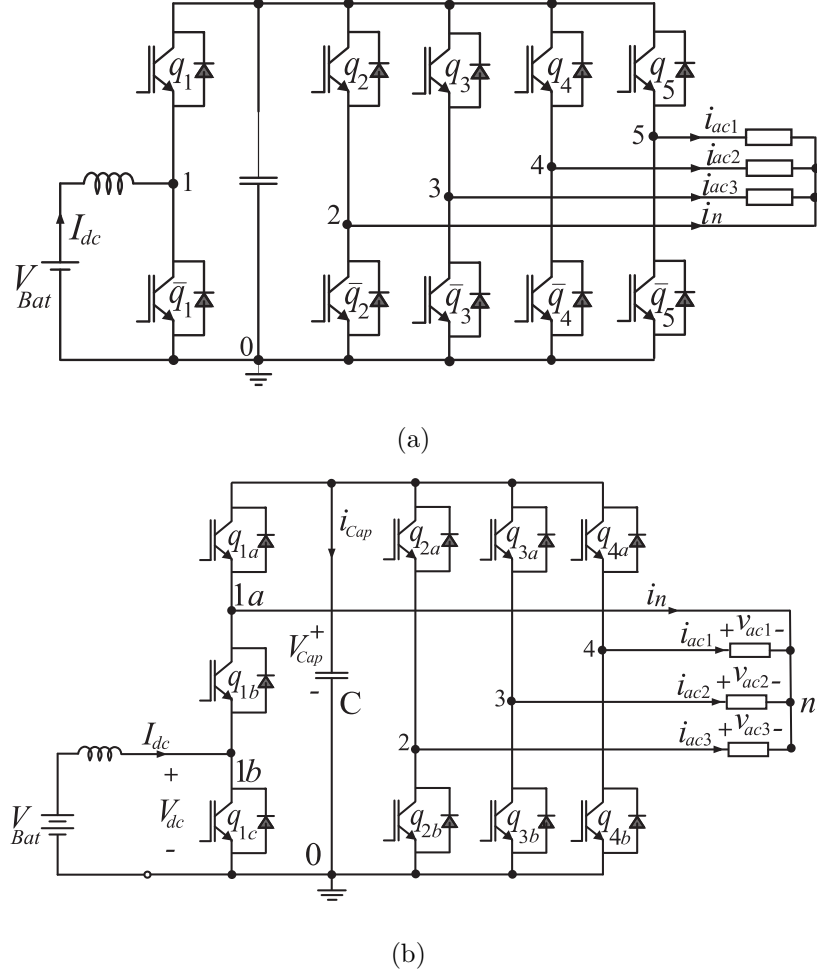


Fig. 4.1. Bidirectional DC-DC-AC converters : (a) conventional solution, and (b) proposed converter.

voltage at point 1a [see Fig. 4.1(b)] than that at point 1b. Table 4.1 shows all possible states with the indication of no-prohibited states.

From Table 4.1 it is possible to write the equations related to the three-leg switch, as follows:

$$v_{1a0} = [q_{1a}(1 - q_{1b}q_{1c})] V_{Cap} \quad (4.1)$$

$$v_{1b0} = [q_{1a}q_{1b}(1 - q_{1c})] V_{Cap} \quad (4.2)$$

where V_{Cap} is the dc-link voltage. For the proposed three-phase four-wire converter, in order to define the voltages at dc and ac converter sides, it is necessary to write

Table 4.1
Prohibited switching states of three-switch leg.

States	q_{1a}	q_{1b}	q_{1c}	Prohibited States
1	0	0	0	Yes
2	0	0	1	Yes
3	0	1	0	Yes
4	0	1	1	No
5	1	0	0	Yes
6	1	0	1	No
7	1	1	0	No
8	1	1	1	Yes

the voltage at the second, third, and fourth legs, (i.e., v_{20}, v_{30}, v_{40}), which are given by:

$$v_{20} = q_{2a}V_{Cap} \text{ or } v_{20} = (1 - q_{2b})V_{Cap} \quad (4.3)$$

$$v_{30} = q_{3a}V_{Cap} \text{ or } v_{30} = (1 - q_{3b})V_{Cap} \quad (4.4)$$

$$v_{40} = q_{4a}V_{Cap} \text{ or } v_{40} = (1 - q_{4b})V_{Cap} \quad (4.5)$$

where q_{2a} , q_{2b} , q_{3a} , q_{3b} , q_{4a} and q_{4b} are the state of the switches in the proposed converter.

Once the voltages v_{1a0} , v_{1b0} , v_{20} , v_{30} and v_{40} are defined, it is possible to write the voltages at dc and ac converter sides, i.e.:

$$v_{dc} = v_{1b0} = [q_{1a}q_{1b}(1 - q_{1c})]V_{Cap} \quad (4.6)$$

$$v_{ac1} = v_{40} - v_{n0} = q_{4a}V_{Cap} - v_{n0} \quad (4.7)$$

$$v_{ac2} = v_{30} - v_{n0} = q_{3a}V_{Cap} - v_{n0} \quad (4.8)$$

$$v_{ac3} = v_{20} - v_{n0} = q_{2a}V_{Cap} - v_{n0} \quad (4.9)$$

where v_{n0} is the voltage of point n referred to the 0, which is given by:

$$V_{n0} = v_{1a0} = [q_{1a}(1 - q_{1b}q_{1c})]V_{Cap} \quad (4.10)$$

4.2 PWM Strategy

The voltages generated at the dc and ac converter sides were obtained for the three-phase four-wire converters as a function of the state of switches, as in (4.6)-(4.9). The goal of the PWM strategy is to define the state of the switches to guarantee that the desired dc and ac voltages will be generated by the converters. The gating signals of the switches must be obtained to avoid the prohibited states (short-circuit or one of the unwanted switching states) of the proposed converters as well as to guarantee independent control at both converter sides. If the desired voltages for the dc and ac converter sides are given respectively by V_{dc}^* and $v_{ac1}^* = V_{ac}^* \cos(\omega t)$,

$v_{ac2}^* = V_{ac}^* \cos(\omega t + 120^\circ)$ and $v_{ac3}^* = V_{ac}^* \cos(\omega t + 240^\circ)$, then the reference voltages from the points 1a, 1b, 2, 3, and 4 to the point 0 may be expressed as:

$$v_{1b0}^* = V_{dc}^* \quad (4.11)$$

$$v_{1a0}^* = V_{offset}^* \quad (4.12)$$

$$v_{20}^* = v_{ac1}^* + V_{offset}^* \quad (4.13)$$

$$v_{30}^* = v_{ac2}^* + V_{offset}^* \quad (4.14)$$

$$v_{40}^* = v_{ac3}^* + V_{offset}^* \quad (4.15)$$

where V_{offset}^* is the voltage to avoid the prohibited states.

The gating signals can be generated comparing modulating reference signals v_{1a0}^* , v_{1b0}^* , v_{20}^* , v_{30}^* and v_{40}^* with a high frequency triangular carrier signal, as depicted in Fig. 4.2(a). Fig. 4.2(b) shows the relationship between THD versus the modulation ratio (m_a). As expected, as far as m_a increases the THD is reduced.

4.3 Control Strategy

Fig. 4.3 presents the control block diagram for the proposed converter. The capacitor voltage V_{Cap} is adjusted to its reference V_{Cap}^* value by using a controller PI_v . This controller provides the amplitude of the reference current I_{dc}^* . The current controller is implemented by using a controller indicated by the block PI_i , which furnishes the voltage V_{dc}^* employed in the PWM scheme presented in Section III. The ac voltages (v_{ac1}^* , v_{ac2}^* and v_{ac3}^*) for the three-phase converter have been obtained in open-loop.

One way to define the gains of the proportional-integral (PI) controller is writing the open-loop $[H(s)]$ and closed-loop $[G(s)]$ transfer functions. Assuming that the converter is an ideal controlled voltage source, the open loop transfer function for the current control is given by:

$$H(s) = \frac{K_i(\frac{K_p}{K_i}s + 1)}{s} \frac{\frac{1}{R}}{\frac{L}{R}s + 1}. \quad (4.16)$$

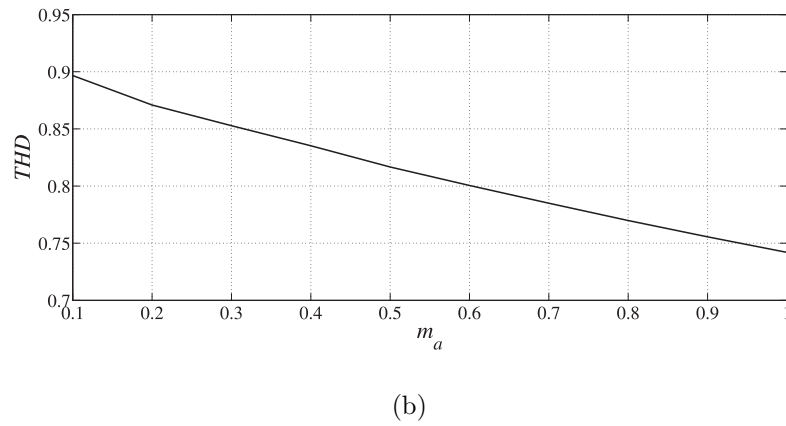
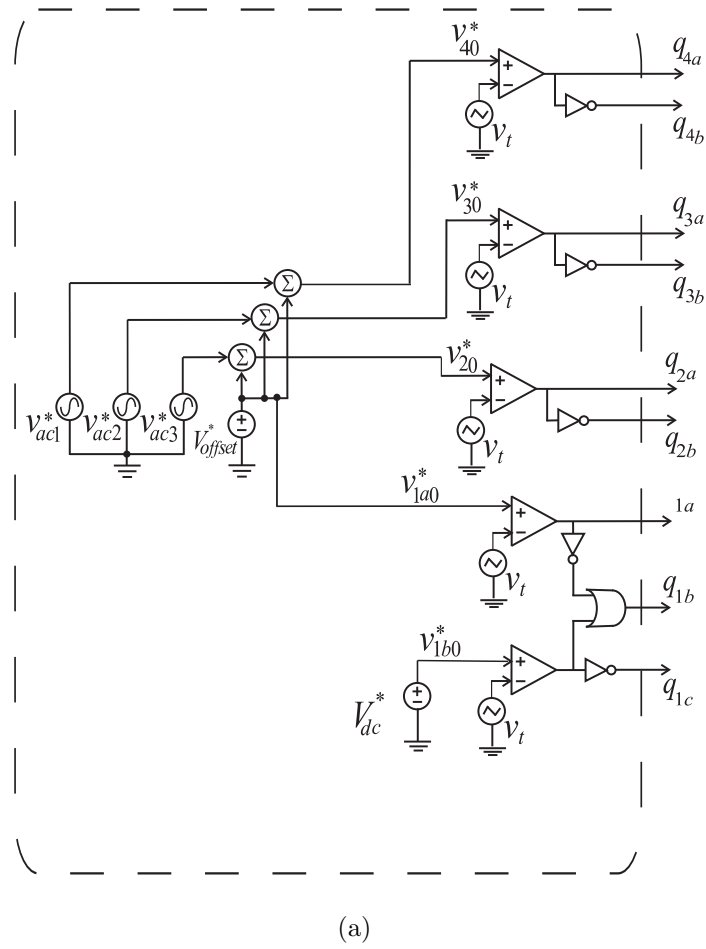


Fig. 4.2. (a) Analog PWM strategy, (b) THD of the output current as a function of m_a .

Canceling the zero of the controller with the pole of the system, the open loop transfer function depends only on the K_i and R as follows:

$$H(s) = \frac{K_i}{Rs} \quad (4.17)$$

since

$$\frac{K_p}{K_i} = \frac{L}{R}. \quad (4.18)$$

The closed-loop transfer function is obtained as below:

$$G(s) = \frac{K_i}{K_i + Rs} \quad (4.19)$$

which means a pole placed at:

$$s = \frac{-K_i}{R} \quad (4.20)$$

Equations (4.19) and (4.20) are enough to find the controller's gains. The design of the gains of the voltage controller can be obtained as presented in [91].

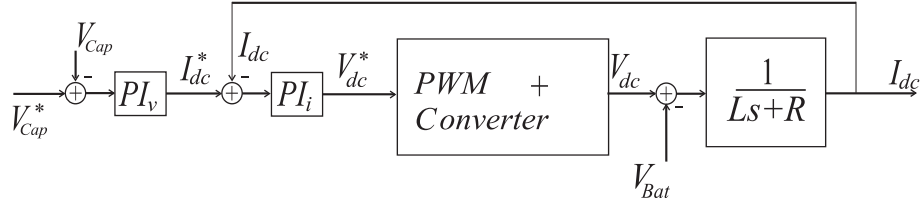


Fig. 4.3. Control block diagram.

4.4 Dc-link Capacitor Variables

The dc-link capacitor current (i_{Cap}) for the conventional and proposed converters can be written respectively as follows:

$$i_{Cap} = q_1 I_{dc} - q_2 i_n - q_3 i_{ac3} - q_4 i_{ac2} - q_5 i_{ac1} \quad (4.21)$$

$$\begin{aligned}
i_{Cap} = & \frac{q_{1a} + q_{1a}q_{1c}}{1 + q_{1a}q_{1c}}I_{dc} - \frac{q_{1a}q_{1b}}{1 + q_{1a}q_{1c}}i_n - q_{2a}i_{ac3} \\
& - q_{3a}i_{ac2} - q_{4a}i_{ac1}
\end{aligned} \tag{4.22}$$

The power losses on the dc-link capacitor can be calculated by:

$$P_{loss}^{Ho} = 0.45ESR_{(100Hz)}(I_{c,rms}^{Ho})^2 \tag{4.23}$$

where $ESR_{(100Hz)}$ is the equivalent series resistance at the frequency of 100Hz, and $I_{c,rms}^{Ho}$ is the high-order root mean square (RMS) of the current on the dc-link for high harmonic component ($h > 50$). As ERS is almost constant for frequency higher than 3KHz, the P_{loss}^{Ho} depends only on the $I_{c,rms}^{Ho}$, which means that the reduction of the power losses on the dc-link capacitor is determined by RMS current.

Fig. 4.4 shows the harmonic spectrum of the dc-link capacitor current. The proposed topology provides the reduction of the high-order harmonic frequencies when compared with a conventional one and consequently the power losses on the capacitor will be lesser.

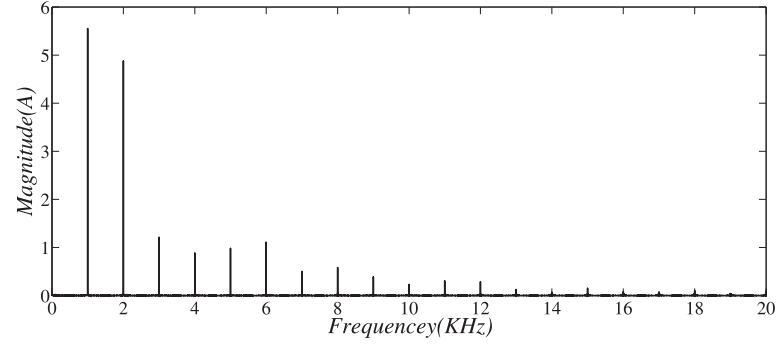
The dc-link capacitor voltage for the proposed converter is larger than that of the conventional one due to the three-switch leg, which requires a V_{offset} (to avoid the prohibited states). In this case dc-link capacitor voltage is defined by the sum of the ac and dc desired voltages.

4.5 Simulated Results

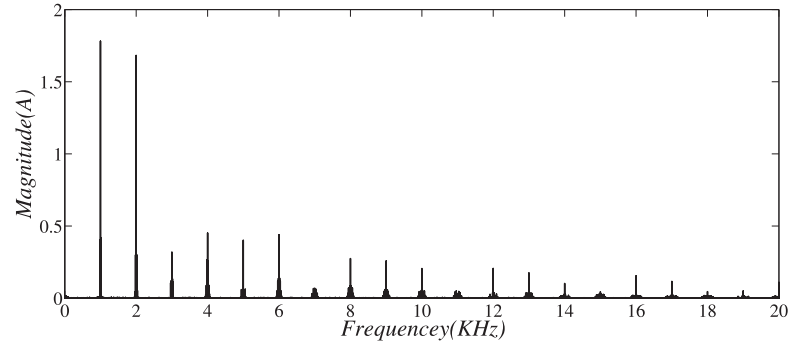
The proposed three-phase four-wire converter has been tested throughout dynamic simulation with PSIM software.

The modulation strategy has been performed in C language by using the DLL block. The simulation results were obtained with the following parameters: $V_{dc} = 45V$ and $f_s = 20KHz$. The inductor and dc link capacitor parameters in the dc side: $L = 2mH$ and $C = 2200\mu F$ also the RL load in the ac side: $R = 10\Omega$ and $L = 3mH$.

Figs. 4.5(a), 4.6, and 4.7 show the simulation results for the three-phase four-wire conventional converter. Fig. 4.5(a) shows the three-phase currents (i_{ac1} , i_{ac2} and i_{ac3}).



(a)



(b)

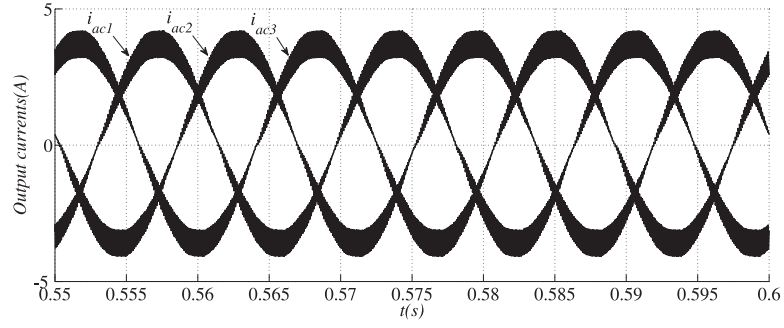
Fig. 4.4. Spectrum of the dc-link capacitor current: (a) conventional and (b) proposed topology.

Figs. 4.6(a)-(c) show the phase voltages (v_{ac1} , v_{ac2} , v_{ac3}). Figs. 4.7(a)-(c) show the line-line voltages ($v_{ac12} = v_{ac1} - v_{ac2}$, $v_{ac13} = v_{ac1} - v_{ac3}$, $v_{ac23} = v_{ac2} - v_{ac3}$).

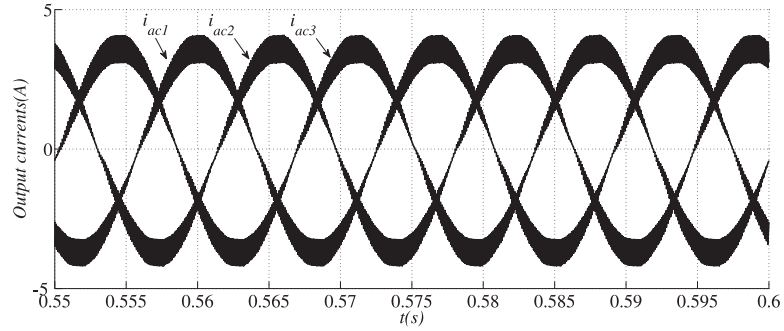
Fig. 4.8(a) shows the reference ($V_{Cap}^* = 155V$) and measured (V_{Cap}) capacitor voltages while the Fig. 4.8(b) illustrates the reference and measured currents which they rich steady state.

Figs. 4.5(b), 4.9, and 4.10 show the simulation results for the three-phase four-wire proposed converter.

Fig. 4.5(b) shows the three-phase currents (i_{ac1} , i_{ac2} and i_{ac3}) which, they are shifted by 120° .



(a)



(b)

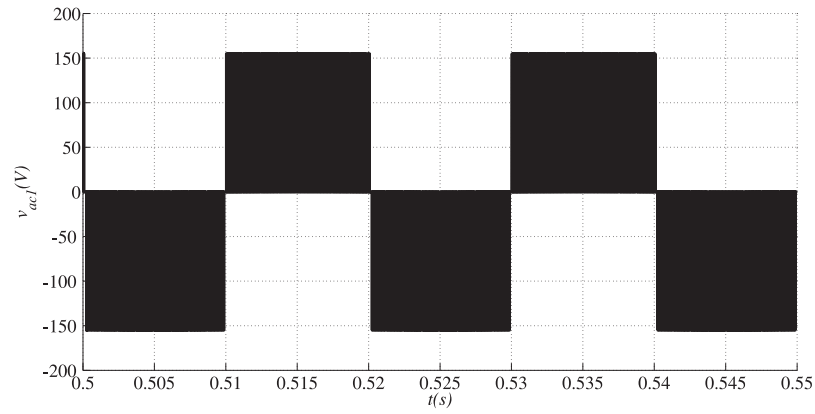
Fig. 4.5. Three-phase ac currents: (a) conventional topology and, (b) proposed topology.

Figs. 4.9(a)-(c) show the phase voltages (v_{ac1} , v_{ac2} , v_{ac3}) and Figs. 4.10(a)-(c) shows the line-line voltages ($v_{ac12} = v_{ac1} - v_{ac2}$, $v_{ac13} = v_{ac1} - v_{ac3}$ and $v_{ac23} = v_{ac2} - v_{ac3}$). The line-line voltages have three levels, because of the pole voltages at point 2, 3 and 4 [see equations (4.3)-(4.5)], are V_{dc} or 0. The phase voltage and the line-line voltage in the four-wire converter are the same and they have 3 levels. According to the equation (4.10), the neutral voltage (v_{n0}) is equal to V_{dc} . Because of this fact the phase voltage has three levels.

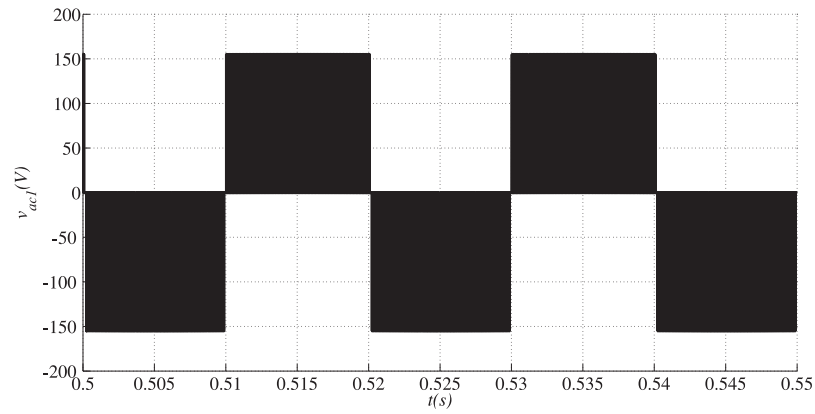
Fig. 4.11(a) illustrates the reference ($V_{Cap}^* = 155V$) and measured (V_{Cap}) capacitor voltages and it is possible to see the transient mode is less than 0.1s and the steady state error is 0 while the Fig. 4.11(b) shows the measured current obtains the steady state in less than 0.2s.

Fig. 4.8(b) shows the reference and measured dc currents for the conventional converter (I_{dc}^* and I_{dc}) and, on the other hand, Fig. 4.11(b) shows the reference and measured dc currents for the proposed converter (I_{dc}^* and I_{dc}). Comparison between both converter, it shows that the controller works good because of the transient mode is less than 0.1s and the steady state error is 0.

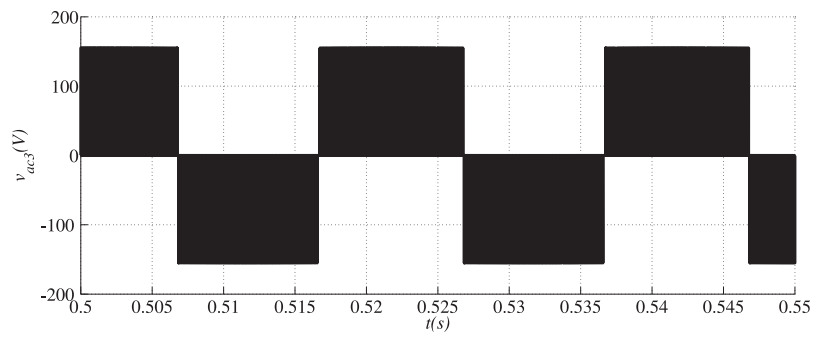
Fig. 4.12(a) shows the transient operation for the reference and measured currents and Fig. 4.12(b) shows the transient operation (load at the ac side being doubled at $t=1.3s$) for the reference and measured capacitor voltages.



(a)

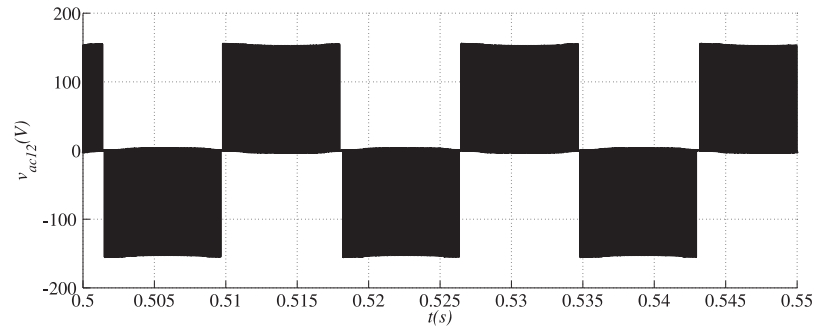


(b)

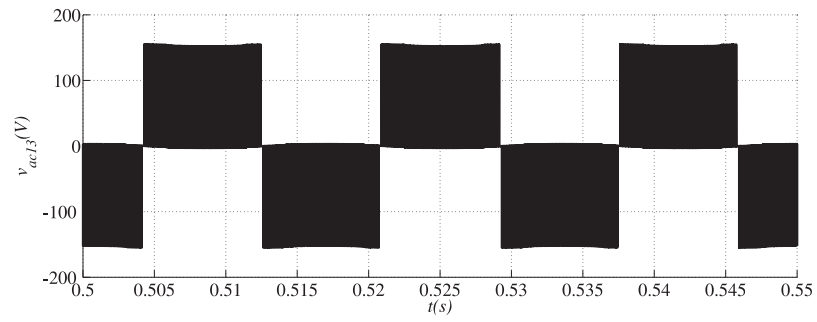


(c)

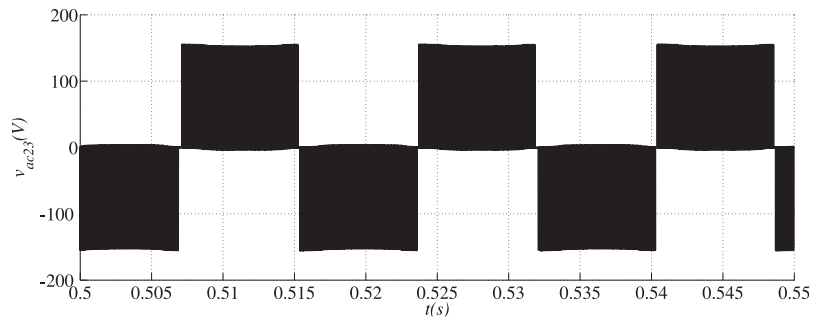
Fig. 4.6. Simulation results for the three-phase conventional converter: (a) phase voltage at phase 1, (b) phase voltage at phase 2, and (c) phase voltage at phase 3.



(a)

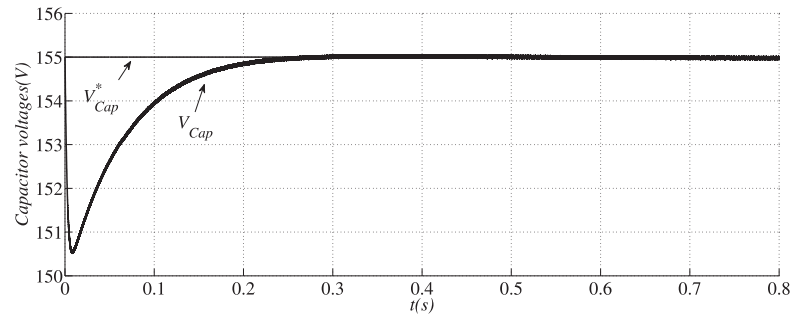


(b)

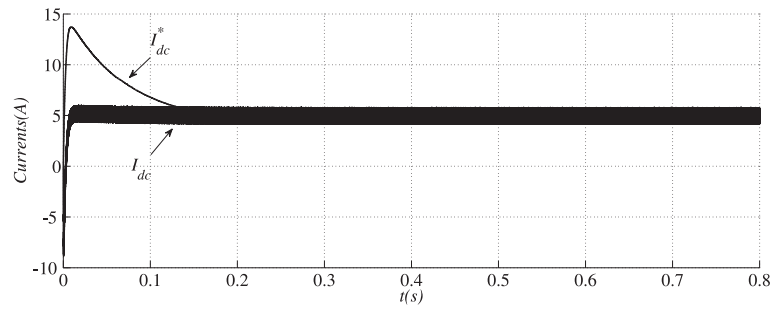


(c)

Fig. 4.7. Simulation results for the three-phase conventional converter: (a) line-line voltage (phase 1-2), (b) line-line voltage (phase 1-3), and (c) line-line voltage (phase 2-3).

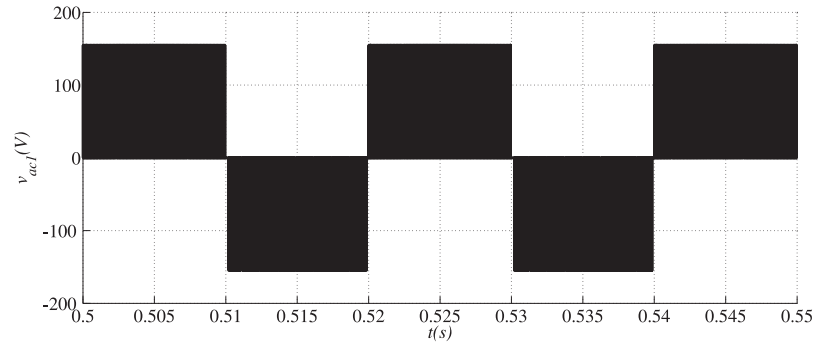


(a)

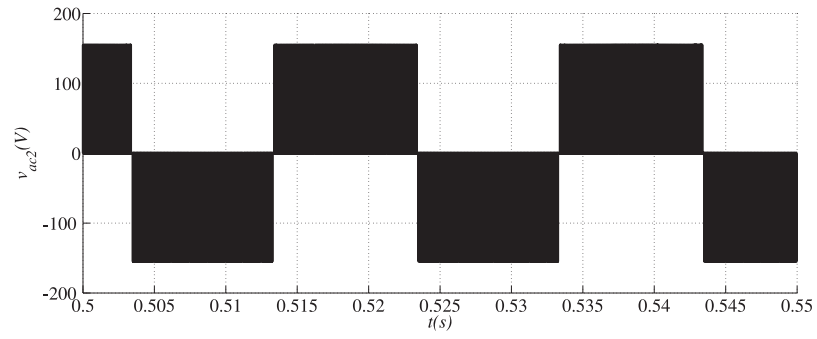


(b)

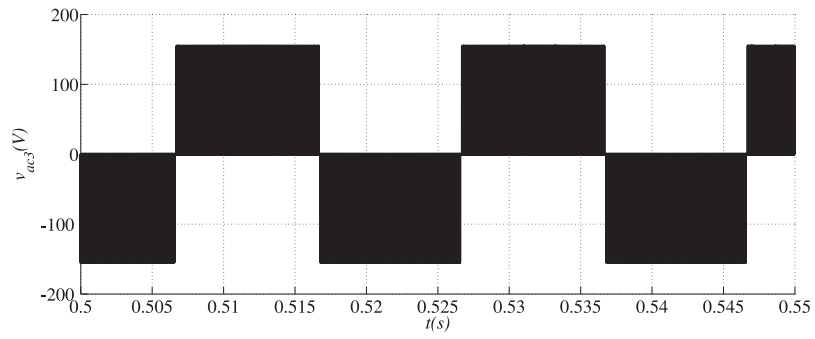
Fig. 4.8. Simulation results for the three-phase conventional converter: (a) reference and measured capacitor voltages, and (b) reference and measured dc currents.



(a)

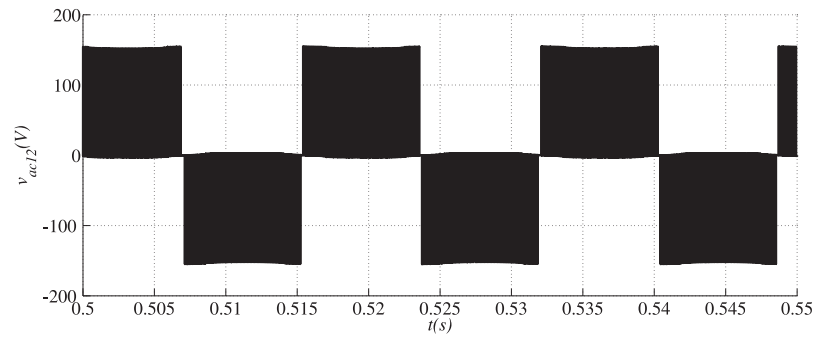


(b)

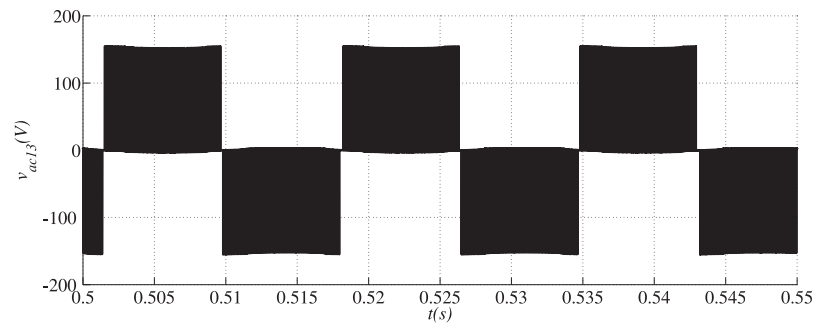


(c)

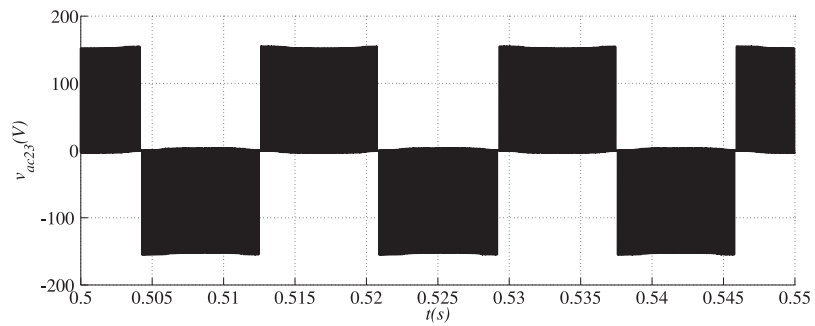
Fig. 4.9. Simulation results for the three-phase proposed converter: (a) phase voltage at phase 1, (b) phase voltage at phase 2, and (c) phase voltage at phase 3.



(a)

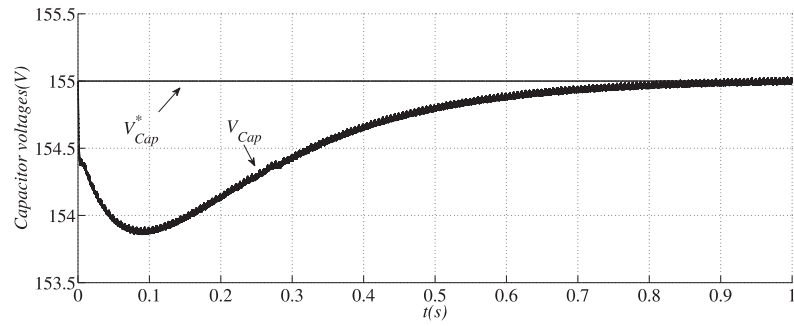


(b)

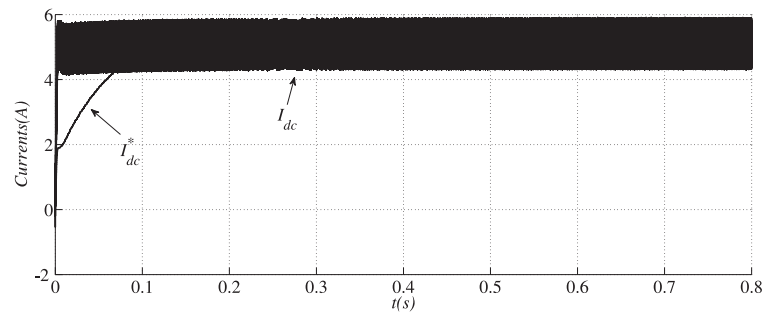


(c)

Fig. 4.10. Simulation results for the three-phase proposed converter: (a) line-line voltage (phase 1-2), (b) line-line voltage (phase 1-3), and (c) line-line voltage (phase 2-3).

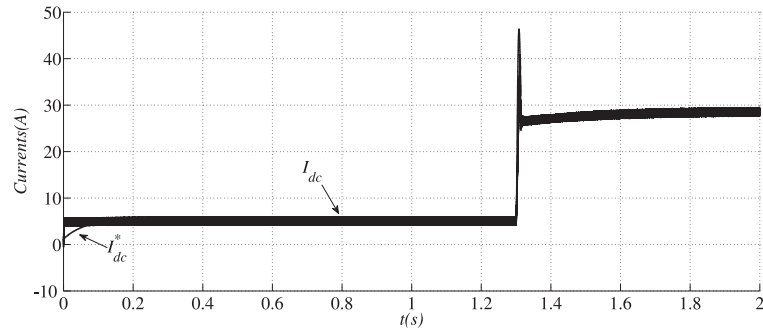


(a)

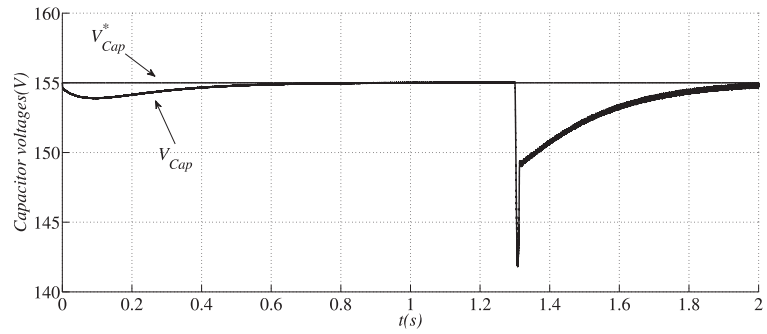


(b)

Fig. 4.11. Simulation results for the three-phase proposed converter: (a) reference and measured capacitor voltages, and (b) reference and measured dc currents.



(a)



(b)

Fig. 4.12. Simulation results for the three-phase converter: (a) transient operation for the reference and measured currents, and (b) transient operation for the reference and measured capacitor voltages .

5. PROOF-OF-CONCEPT EXPERIMENTAL SETUP

This chapter presents the experimental setup, which includes the DSP, the Drivers & Integrating Board power, Power Converter & Heat-Sink, and experimental outcomes.

5.1 DSP

The experimental result in this thesis is obtained by using the eZdsp starter kit TMS320F28335 as depicted in Fig. 5.1, which is from the Texas Instrument company (TI). The starter kit includes the JTAG emulator, F28335 target board, 128Kx16 asynchronous SRAM. Application of starter kit for this research is to generate the 12 dependent and independent PWMs to control the power switches. The DSP connects to the computer via the USB connector and power is supplied from the grid via the power connector which converts the grid voltage to 5 Volts. The starter kit programmed by the Code Composer Studio software (V3.3) which includes the C compiler, assembler, linker and real-time debug support. Figs. 5.2 and 5.3 show the compiling steps for the program. The steps are expressed as:

- The starter kit must be connected to the computer and turned on.
- Choose Setup CCstudio V3.3 in order to add ezDSP as depicted in Fig. 5.2(a).
- From the Debug pull-down menu, choose connect as depicted in Fig. 5.2(b).
- From the Project pull-down menu, choose open as depicted in Fig. 5.2(c).
- Build the project from the Project pull-down menu, as depicted in Fig. 5.3(a).
- From the File pull-down menu, choose the Load Program option and after selecting Debug, choose the file with (.out) extension as depicted in Fig. 5.3(b).

- Select the Run from the Debug pull-down menu, as shown in Fig. 5.3(c).



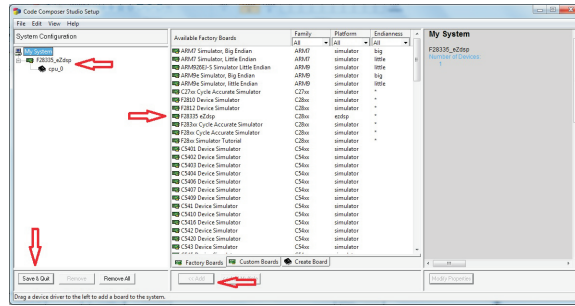
Fig. 5.1. Photo of the Printed Circuit Board for the starter kit.

When the program starts running, it is possible to see the PWM signals on the oscilloscope. The connector P8 is defined by the GPIOs location. The DSP has the ability to generate 6 PWMs and each PWM has a port A and a port B which means the port A could be complementary of the port B. For instance, to generate PWMs for a conventional three-phase dc to ac converter, it is necessary to generate three PWMs. EPWM 1 includes the first phase signal, EPWM 2 includes the second phase signal, and EPWM 3 includes the third phase signal. Below indicates the code related to the three switches for the first leg for the proposed converter:

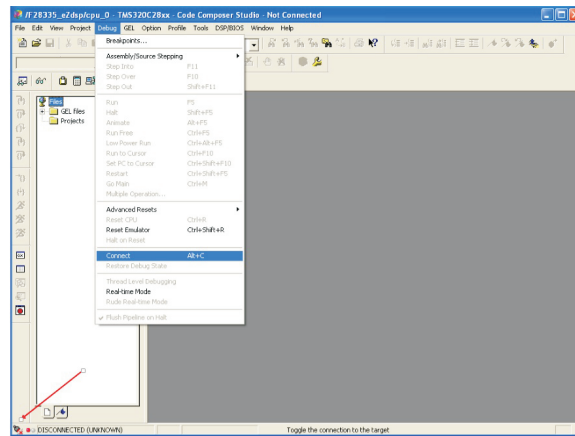
- Define the reference voltages:

$$Vs1_{ref} = 0.4m_a \sin(teta) + 0.6 \quad (5.1)$$

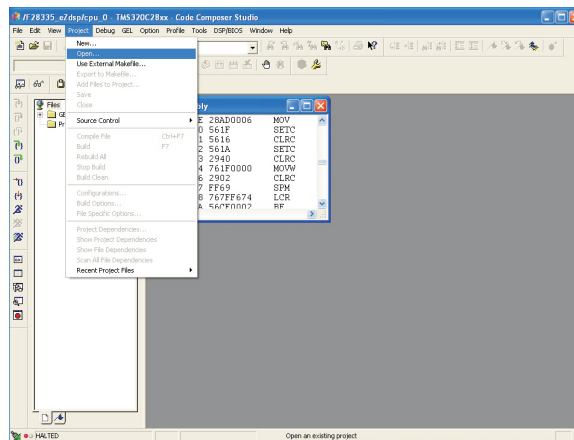
$$Vs2_{ref} = 0.2 \quad (5.2)$$



(a)



(b)



(c)

Fig. 5.2. Spectrum of code composer: (a) code composer studio setup, (b) connect the board and (c) open the project.

- Define the GPIOs on the P8 connector:

$$EPwm1Regs.CMPA.half.CMPA = Vs1_{ref} \times 7500 \quad (5.3)$$

$$EPwm1Regs.CMPB = Vs2_{ref} \times 7500 \quad (5.4)$$

$$EPwm2Regs.CMPA.half.CMPA = Vs1_{ref} \times 7500 \quad (5.5)$$

$$EPwm2Regs.CMPB = Vs2_{ref} \times 7500 \quad (5.6)$$

For the first leg which includes three switch in the proposed converter, it is necessary to generate an independent signal, which means to generate the inverse of the signal. The generation of inverse signal expressed as:

- For the IGBT A the first event should start from 1 which is defined by AQ_{SET} :

$$EPwm1Regs.AQCTLA.bit.ZRO = AQ_{SET} \quad (5.7)$$

$$EPwm1Regs.AQCTLA.bit.CAU = AQ_{CLEAR} \quad (5.8)$$

- And respectively for the IGBT B to generate the inverse of the first signal, the first signal should start from 0 which is defined by AQ_{CLEAR} :

$$EPwm1Regs.AQCTLA.bit.ZRO = AQ_{CLEAR} \quad (5.9)$$

$$EPwm1Regs.AQCTLA.bit.CAU = AQ_{SET} \quad (5.10)$$

5.2 Drivers & Integrating Board

This section presents the function of the driver, the basic board and the integrated board. The 2SC0108T dual driver as depicted in Fig. 5.4 is designed for the universal application because of its high reliability. The driver can support the IGBT up to 600A/1200V or 450A/1700V. The 2SC0108T driver is a low cost driver and it is applicable for DC-DC & DC-AC converters and it has a capability to protect the system from the short-circuiting.

Among the proposed converters the ability of this driver is to generate the half-bridge mode and direct mode signals. While using the half-bridge mode it is enough to generate just one PWM, and the driver will generate the complementary of the signal. On the other hand, in direct mode the signals are independent and it is possible to send two independent signals to the driver. Fig. 5.5(a) shows the interface of the primary side of the driver which is connected to the DSP. Fig. 5.5(b) shows the secondary side of the driver which is connected to the power IGBTs modules.

The 2SC0108T driver is attached on the basic board 2BB0108T which is depicted in Fig. 5.6. The basic board 2BB0108T is the suitable dual channel board which can support the IGBT modules up to 1700V. The driver is attached on the basic board and the primary side and secondary side of the basic board should connect to the DSP and the IGBT modules.

In Fig. 5.7, the Electrical interface X3 shows the interface of the primary side that should connect to the DSP and power supply. Power Supply should connect to the VCC (15V). PWM signals which are generated by the DSP should connect to the channel X3. The ground of the basic board should connect to the ground of power supply and ground of the DSP. Pin mode of the primary side, explains the mode of the driver. If the mode is connected to the ground, the half-bridge mode is applied to the driver and if the pin mode is floated, the direct mode is applied to the driver. In Fig. 5.7, the electrical interfaces X1 & X2 show the secondary side of the driver, which are connected to the IGBT modules. The electrical interface X2 and X3 have 3 pins which are defining by the collector, the gate and the emitter. These pins should connect to the collector, the gate and the emitter of the IGBT modules.

Fig. 5.8, shows the proposed printed circuit board in order to use less wire. Between the DSP, power supply and driver there are lots of connection, which they need to connect with the wire, but with the integrated circuit board which is designed in the ultiboard software from the National Instrument company, it is possible to use less wire in the system.

5.3 Power Converter & Heat-Sink

This section presents the power side of the system which is constituted by IGBT modules, a heat-sink, a dc-link capacitor, snubber capacitor and the three-phase load. BSM75GB60DLC is a IGBT module from the EUPEC company which is implemented as a switch in the experimental setup. Collector-emitter voltage(VCE) is up to 600 volts and the collector current at 75 °C is up to 75A and at 25 °C is up to 100A. Fig. 5.9(a) shows the spectrum of the collector, emitter and gate for each switch. BSM75GB60DLC is constituted by two switches. The Signals for the collector, emitter and gate come from the basic board that is explained in previous section. According to Fig. 5.7 the interfaces X1 and X2 respectively relate to channel 1 and channel 2. Channel 1 is related to one switch and channel 2 is related to the other switch in the IGBT modules. It does not matter whether, the channel 1 and channel 2 connect to the bottom switch or upper switch but it is important to know that the points 1,6,7 on the IGBT module should connect to the channel 1 or channel 2 and on the other hand the points 3,4,5 should connect to the other switch.

The power for the IGBT modules supplied from the DC or AC source depends on the application. The proposed converters convert the DC to AC, so the power for the switches supplied from the DC source is as depicted in Fig. 5.9(b). Fig. 5.9(c) shows the snubber capacitor which is used to avoid the high variation of the voltage($\frac{dv}{dt}$). There are two ways to attach the snubber capacitor to the system. If the high derivation voltage is too much it is better to attach one snubber capacitor per switch. The second way is to attach one snubber capacitor per leg if the derivation of the voltage is medium.

Fig. 5.10(a) shows the dc-link capacitor which is storing the voltage. The dc-link capacitor also helps prevent the switching network from oscillating at an inappropriate moment.

When the power comes to the switches, the temperature rises. To avoid the failure in the system, the power IGBTs must attach on the heat-sink which is $36cm \times 14cm \times 4cm$ as depicted in Fig. 5.10(b).

Fig. 5.10(c) shows the three phase load induction motor which is powered by the DC source. The induction motor is an AC motor which needs the AC current for the rotor. The AC current is generated from the DC current that came to the converter and converted to the AC current.

5.4 Experimental Outcomes

This section presents the experimental results for the three-phase and three-phase four-wire power converters. In order to obtain the result for the three-phase proposed converter, there are some steps expressed as:

- Turn the DC source on.
- Connect the DSP to the computer and plug it into the grid.
- Plug the power supply into the grid.
- Run the program from the Code-Composer.
- Start slowly to increase the power from the DC machine.

The parameters for the experimental setup are described as:

$F_s = 10KHz$, $V_{dc} = 40V$, sinusoidal frequency is 10Hz and the load is the three-phase machine.

5.4.1 Three-phase Power Converter

Fig. 5.11(a) shows the PWM for the three switches, which are in the first leg, which can not be turned on simultaneously. Equations below show the reference signals for the three phase PWM.

$$Vs1_{ref} = m_a 0.4 \sin(\theta) + 0.6 \quad (5.11)$$

$$Vs2_{ref} = 0.2 \quad (5.12)$$

$$Vs3_{ref} = m_a 0.4 \sin(\theta + 120) + 0.6 \quad (5.13)$$

$$Vs4_{ref} = m_a 0.4 \sin(\theta + 240) + 0.6 \quad (5.14)$$

The Figs. 5.11(b)-(c) show the schematic of the proposed three-phase converter. Figs. 5.12(a)-(d) show the voltages and the phase currents. Fig. 5.13(a) shows the dc current and voltage between point 1a and the ground. Fig. 5.13(b) shows the line-line voltage between the top line and the middle one and, in addition, shows the top phase current. Fig. 5.13(c) shows the bottom phase voltage and current.

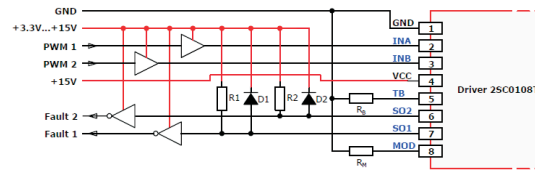
5.4.2 Three-phase Four-wire Power Converter

Fig. 5.14, Fig. 5.15 and Fig. 5.16 show the experimental results for three-phase with four-wire power converter. Fig. 5.14(a) illustrates the line-line voltage and the phase current, while the Fig. 5.14(b) illustrates the average of them. On the other hand, Fig. 5.15(a) illustrates the phase voltage phase current and Fig. 5.15(b) shows the average of them. The comparison between Fig. 5.14(a) and Fig. 5.15(a) validates that the line-line voltage and phase-voltage have three levels as shown in the previous chapter.

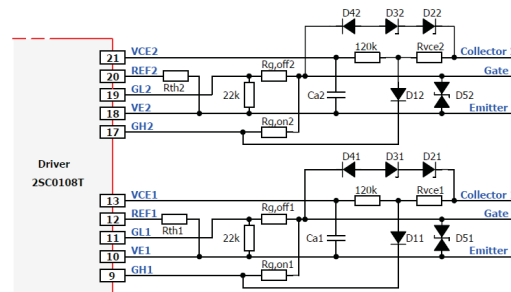
finally, Fig. 5.16(a) shows the input dc voltage while the Fig. 5.16(b) shows the phase current.



Fig. 5.4. Driver 2SC0108T.



(a)



(b)

Fig. 5.5. Spectrum the 2SC0108T driver sides: (a) Primary side, (b) Secondary side.

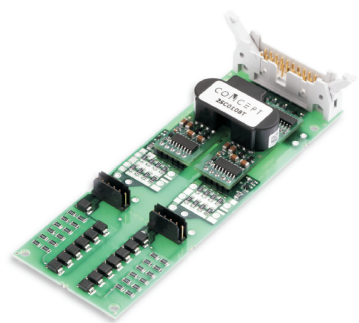


Fig. 5.6. Basic board 2BB0108T.

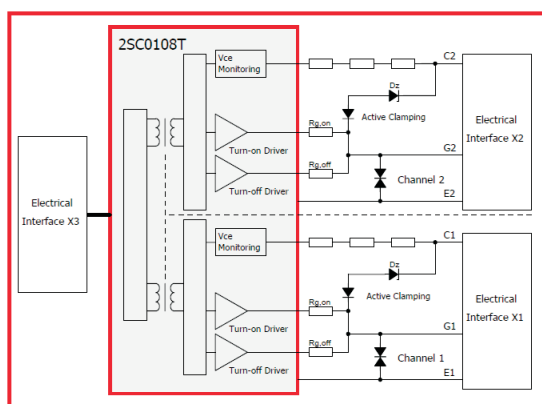


Fig. 5.7. Primary and Secondary sides of the basic board 2BB0108T.

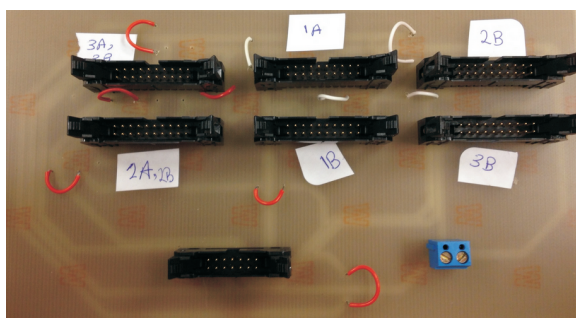
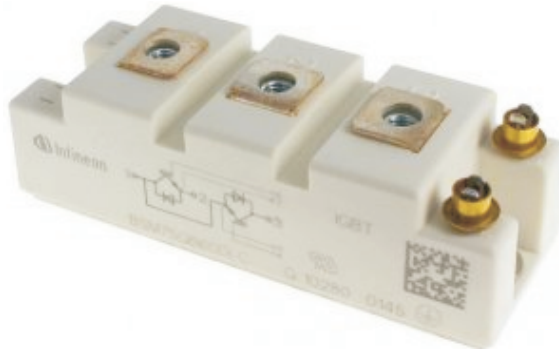
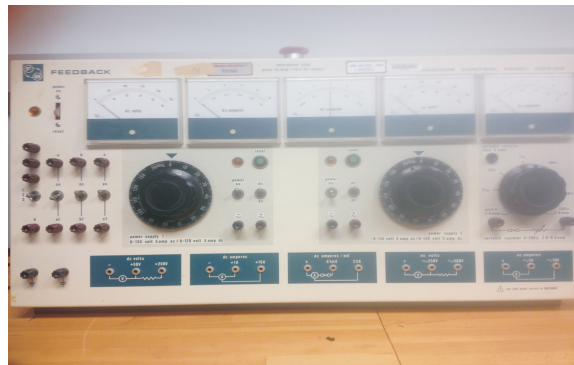


Fig. 5.8. Integrated board.



(a)



(b)

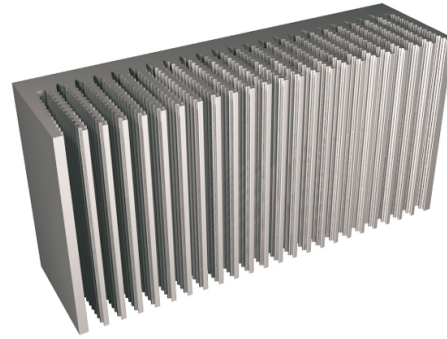


(c)

Fig. 5.9. Spectrum of power parts: (a) BSM75GB60DLC IGBT module, (b) DC source and (c) Snubber capacitor.



(a)

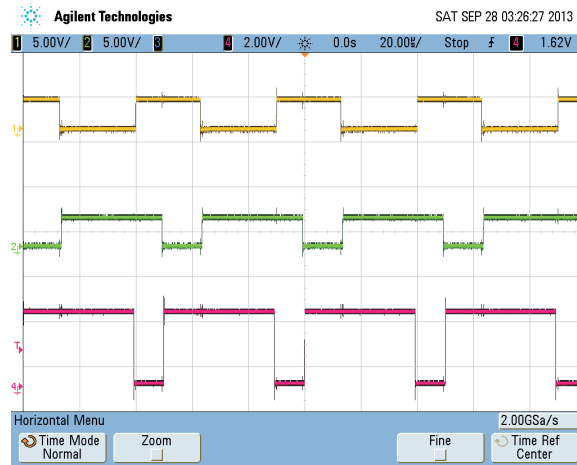


(b)

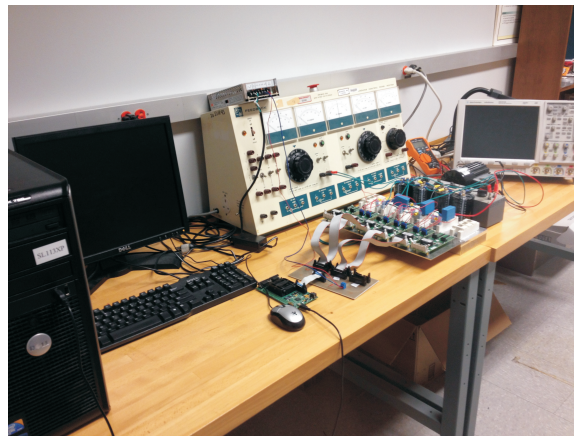


(c)

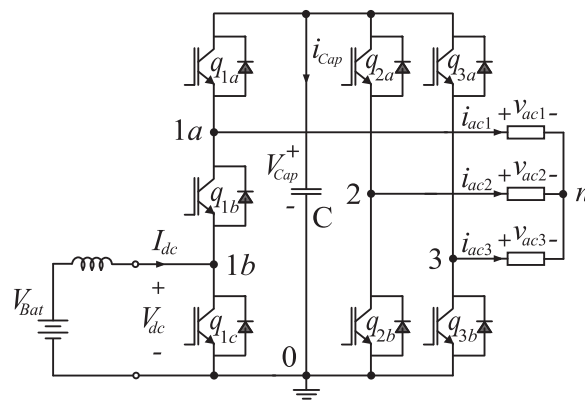
Fig. 5.10. Spectrum of power parts: (a) Dc-link capacitor, (b) Heat sink and (c) Three-phase load.



(a)



(b)



(c)

Fig. 5.11. (a), PWM for the leg with three switches, (b) and (c) Proposed three-phase converter.

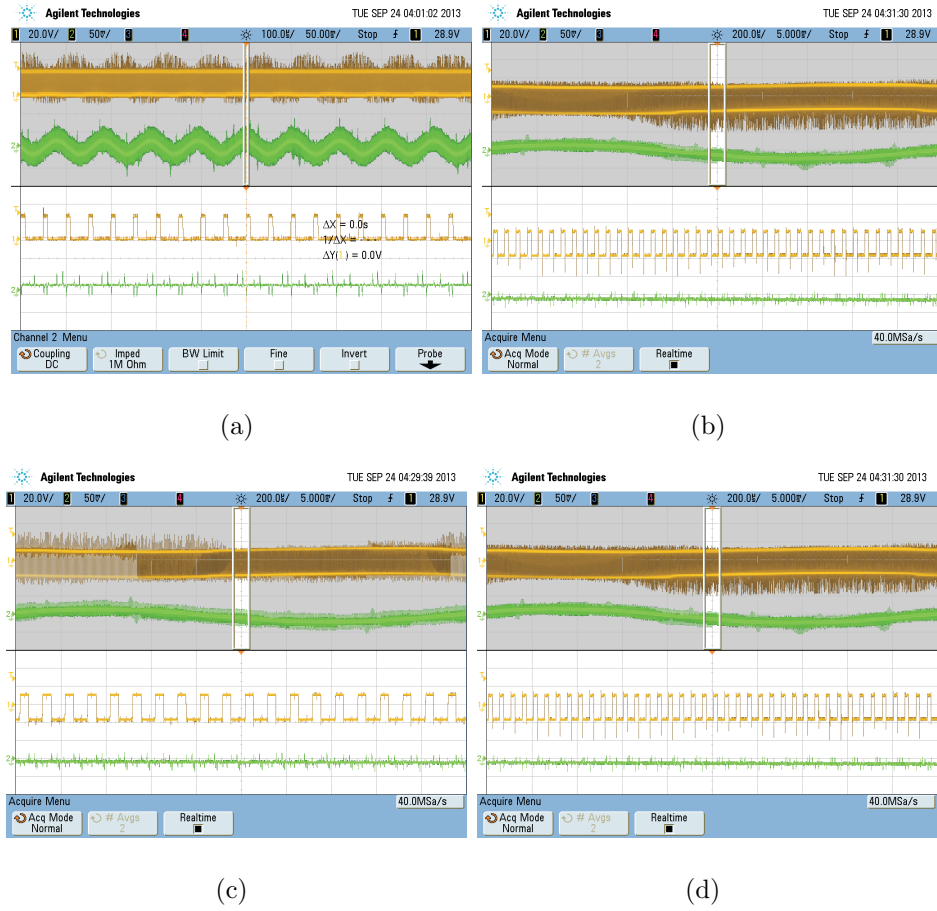
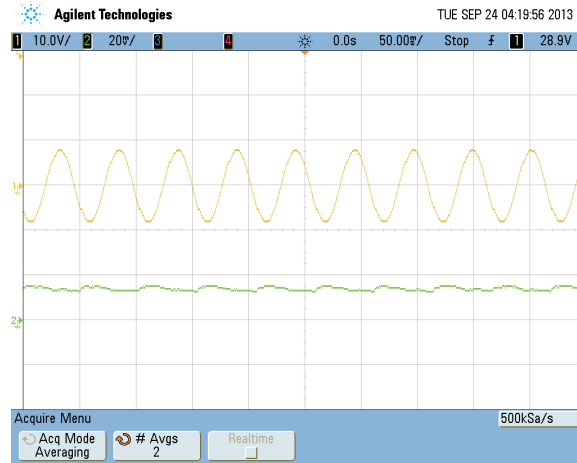
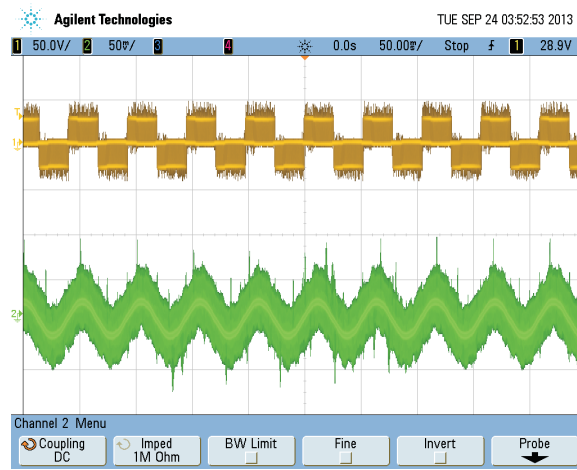


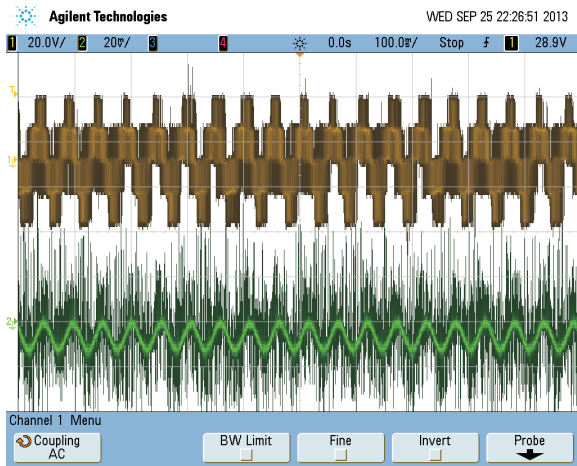
Fig. 5.12. Experimental results for proposed three-phase converter: (a) v_{1b0} and i_{ac1} , (b) v_{1a0} and i_{ac1} , (c) v_{20} and i_{ac2} , and (d) v_{30} and i_{ac3} .



(a)

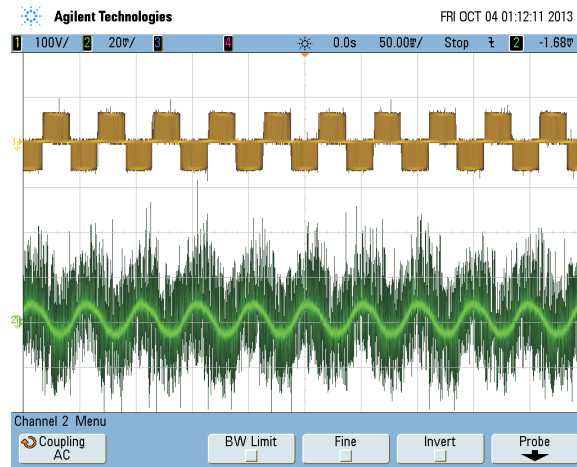


(b)

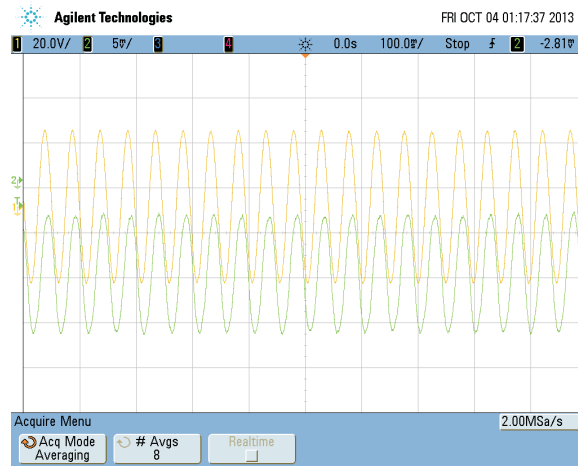


(c)

Fig. 5.13. Experimental results for three-phase proposed converter: (a) v_{1a0} and I_{dc} , (b) v_{1a2} and i_{ac1} and (c) v_{ac3} and i_{ac3} .

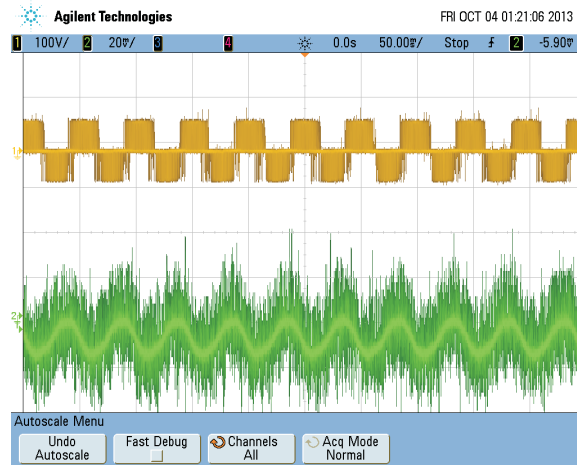


(a)

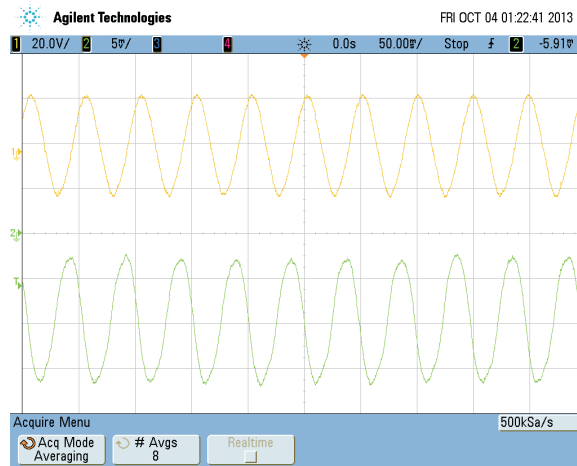


(b)

Fig. 5.14. Experimental results for three-phase with four-wire converter: (a) line-line voltage v_{13} and phase current i_{ac1} and (b) average of the current and voltage

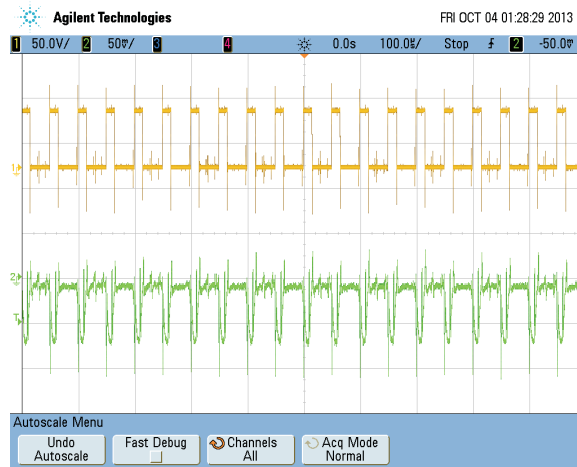


(a)

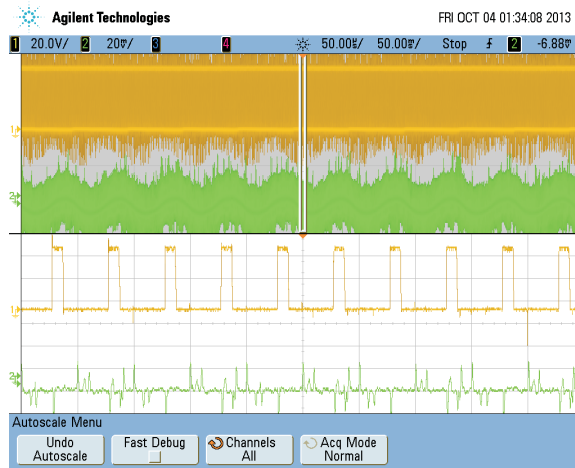


(b)

Fig. 5.15. Experimental results for three-phase with four-wire converter: (a) phase voltage v_{ac1} and phase current i_{ac1} (b) average of the voltage and current



(a)



(b)

Fig. 5.16. Experimental results for three-phase with four-wire converter: (a) V_{1b0} and the i_{1a-1b} and (b) V_{1b0} and the phase current i_{ac1}

6. CONCLUSIONS & FUTURE WORK

6.1 Conclusions

This thesis proposed a bidirectional DC-DC-AC converter for single-phase, three-phase and three-phase four-wire applications. Such power electronics solutions guarantee: (i) bidirectional power flow between dc and ac converter sides, (ii) controllability in both converter sides, (iii) high level of integration, (iv) implementation of two stages (DC-DC and DC-AC) using a unique power conversion stage and (v) reduction of the capacitor losses.

For the control part of the systems, the cascade controller implemented into the system to control the input current and dc-link voltage.

For the single-phase bidirectional converter, one of the switches reduced and additionally, the dc-link capacitor losses reduced, while the converter has the same features as the conventional one.

In three-phase bidirectional power converter, besides of the reducing one switches and the dc-link capacitor losses, by adding the v_{μ}^* to the reference voltage ($0 \leq \mu \leq 1$), it is possible to have 15% more voltage at the dc-link.

Three-phase four-wire power converter is proposed to have access for three-phase terminals and additionally to have access to the neutral point. In this converter like the single-phase and three-phase power converters, one of the switches reduce besides the dc-link capacitor losses reduce. In all the converters total harmonic distortion (THD) is reduced compared the conventional ones.

Finally, with the experimental setup, the experimental results validate the simulation result and theoretical logic which are applied to the proposed converters.

6.2 Future Work

The research produced on this thesis can be further developed in future studies dealing with:

- Implementation of the controller for the experimental setup. In this work the experimental outcomes include the open loop operations, by adding sensors and controllers, it is possible to implement the controller for the systems.
- Implement the controller for the ac side of the proposed systems. In this thesis, input current and dc-link voltage controlled by the PI controllers. The output control strategy is more complex because of the output is a ac variable and it requires more research to apply the controller for this part.
- Calculate the losses for the proposed systems and compare to the conventional solutions. Due the lack of the time, it was not possible to calculate the system losses. In future it may be possible to see the losses of the system and compare it by the conventional solutions. Although there is a reasonable indicative that the losses will be lesser for the proposed systems due to the reduction of one power switch.
- Test the system operation while connected to the grid. It may be possible to connect the system into the grid and see the behavior of the system while the system is connected to the high voltage.
- Test how the system manages the energy while the battery is charged or discharged. For instance it is possible to test, while the system is connected to the grid, see how the system acts when the energy comes from the grid to the battery and when the energy goes from the battery to the grid while it is full.
- Calculate the final price of the proposed systems and compare with the conventional solutions. By reducing one switch and its driver, the final price should be calculated and compared to the conventional solutions.

- Find the operation limits and determine a design tool for the proposed converter.

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